# ASUS CONFIDENTIAL

**MODEL NAME :** ***Elsa***

**PCB NO :** ***???***

**ASUS P/N :** ***???***

# Lanai UMA Schematics Document

## uFCPGA Mobile Merom
## Intel Crestline-GM + ICH8M

2007-03-19

**REV :1.2(DELL: X02)**

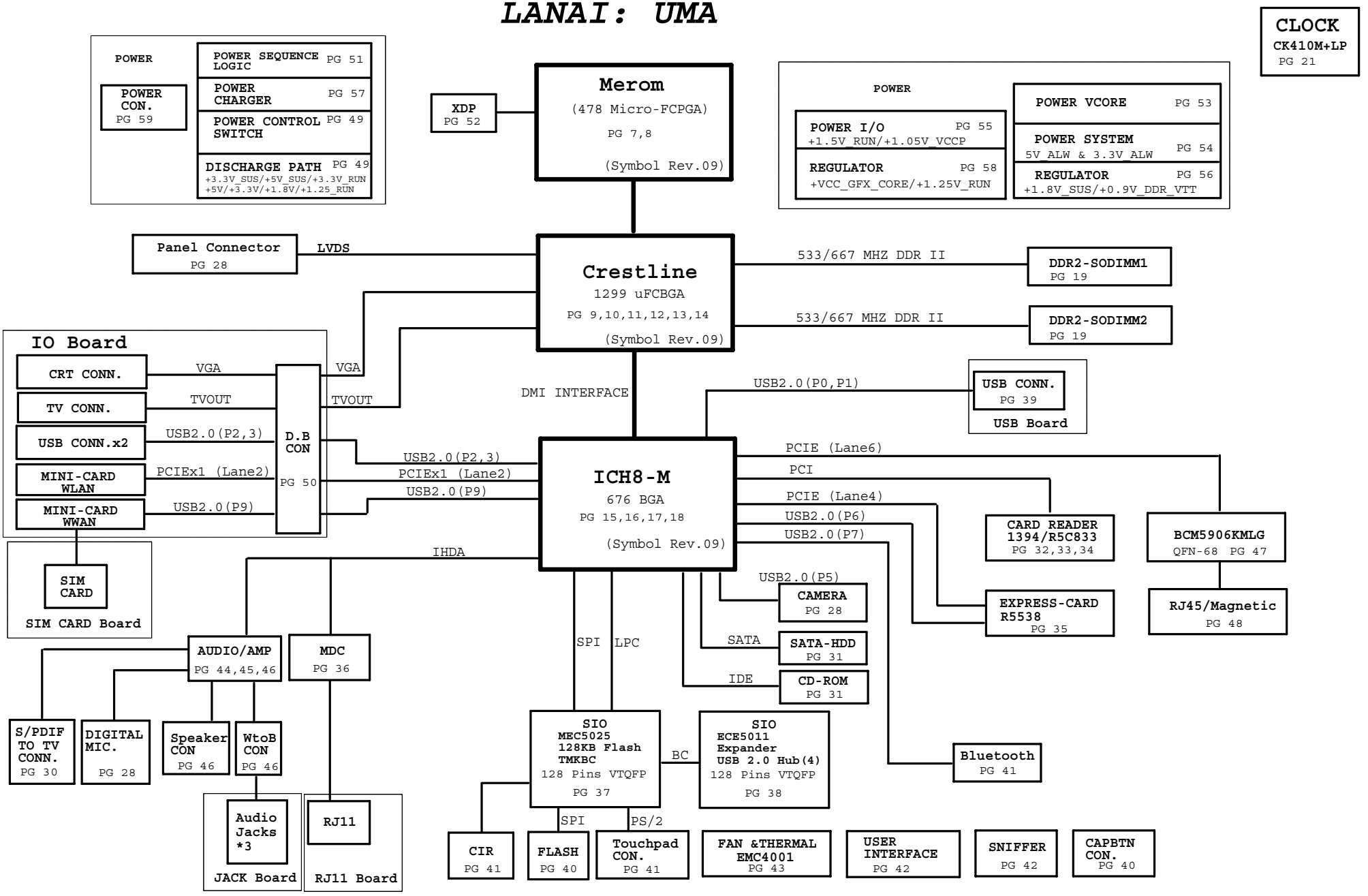
MB PCB

| Part Number | Description |
|---|---|
| DA800004H0L | PCB 00B LA-3071P REV0 M/B |

***BOM NO. ???***
***PCB P/N: ???***

| PROJECT: | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | 1.2 | SHEET 1 OF 68 | Cover Page | RELEASE DATE : | | |

# LANAI: UMA




| PROJECT: | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | DESIGN ENGINEER : |
|---|---|---|---|---|---|
| | 1.2 | SHEET 2 OF 68 | BLOCK DIAGRAM | RELEASE DATE : | |

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| 66 | Modem board change List | |
| 67 | USB board cover page | |
| 68 | USB PORT ( SINGLE * 2 ) | |

## Footprint Definition

| | |
|---|---|
| Resistor | Footprint is 0402 if there is no description |
| Capacitor | Footprint is 0402 if there is no description |
| Ferrite Bead | Footprint is 0603 if there is no description |

## Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

## PCI TABLE

| PCI DEVICE | IDSEL | REQ#/GNT# | PIRQ |
|---|---|---|---|
| R5C833 | PCI_AD17 | PCI_REQ1#<br>PCI_GNT1# | PCI_PIRQC#<br>PCI_PIRQD# |
| | | | |

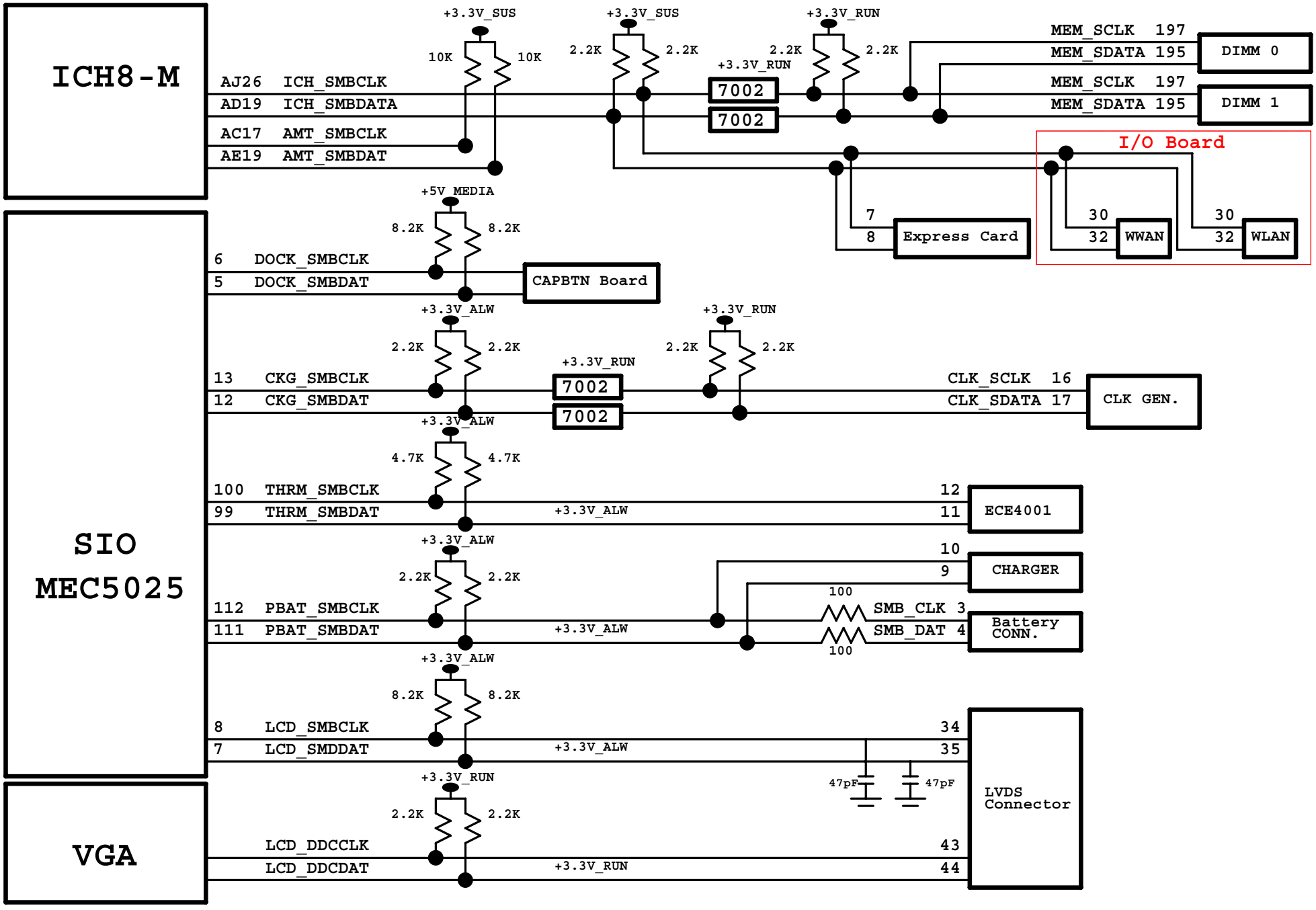
## PCI Express TABLE

| | |
|---|---|
| Lane 1 | WWAN / Mini Card |
| Lane 2 | WLAN / Mini Card |
| Lane 3 | |
| Lane 4 | ExpressCard |
| Lane 5 | |
| Lane 6 | LAN BCM5906KMLG |

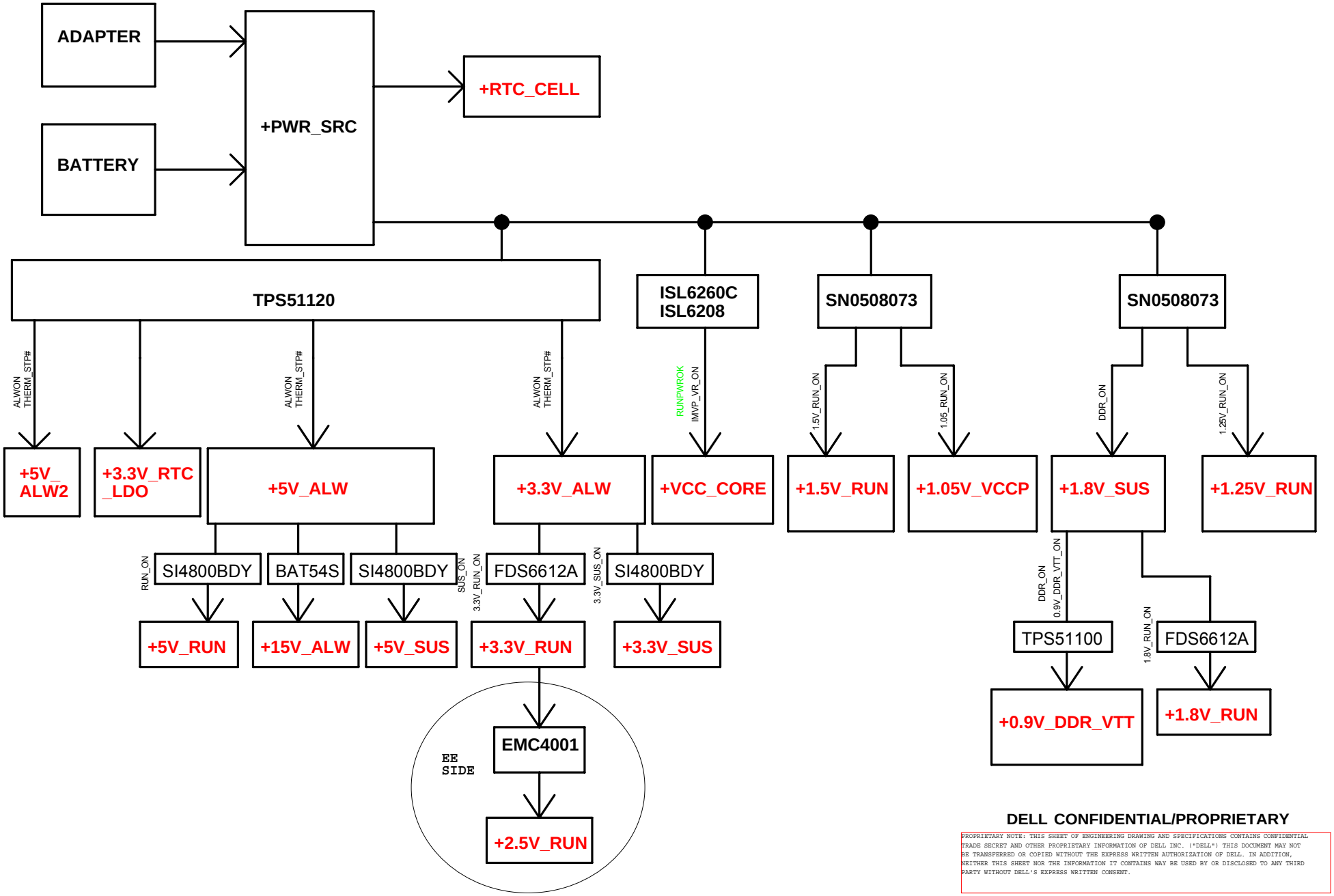
## USB TABLE

| | |
|---|---|
| ICH8-0 (EHCI#1) | User1 (Single port , in USB BD) |
| ICH8-1 (EHCI#1) | User2 (Single port , in USB BD) |
| ICH8-2 (EHCI#1) | User3 (Dual port-bottom , in I/O BD) |
| ICH8-3 (EHCI#1) | User4 (Dual port-top , in I/O BD) |
| ICH8-4 (EHCI#1) | |
| ICH8-5 (EHCI#1) | Camera |
| ICH8-6 (EHCI#2) | ExpressCard |
| ICH8-7 (EHCI#2) | BT Module |
| ICH8-8 (EHCI#2) | |
| ICH8-9 (EHCI#2) | WWAN / Mini Card |

Note : No USB for WLAN



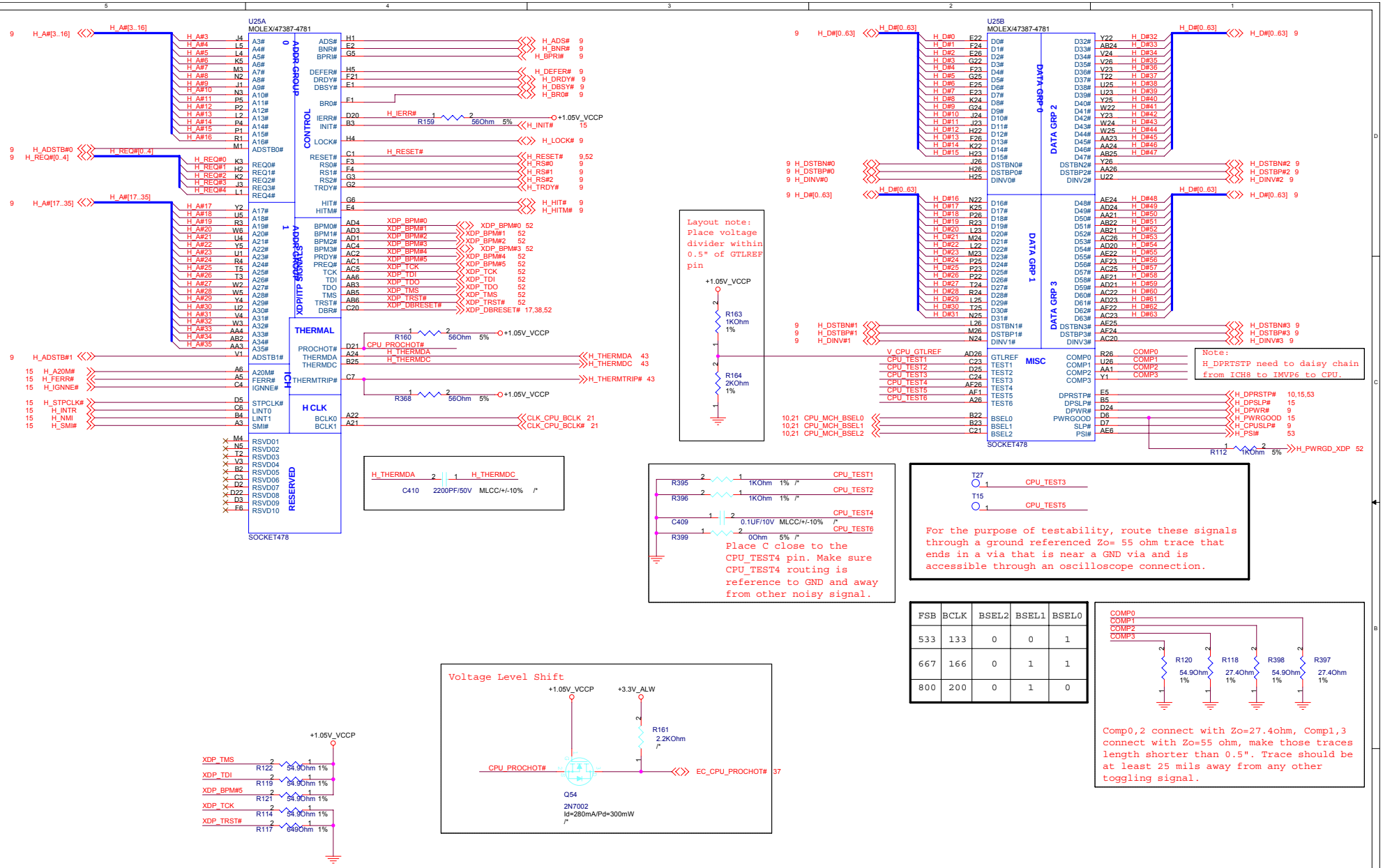

| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION 1.2 | DATE: Monday, March 19, 2007 | DESCRIPTION: *SMBUS BLOCK* | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
| | | SHEET 5 OF 68 | | RELEASE DATE : | | |




**DELL CONFIDENTIAL/PROPRIETARY**

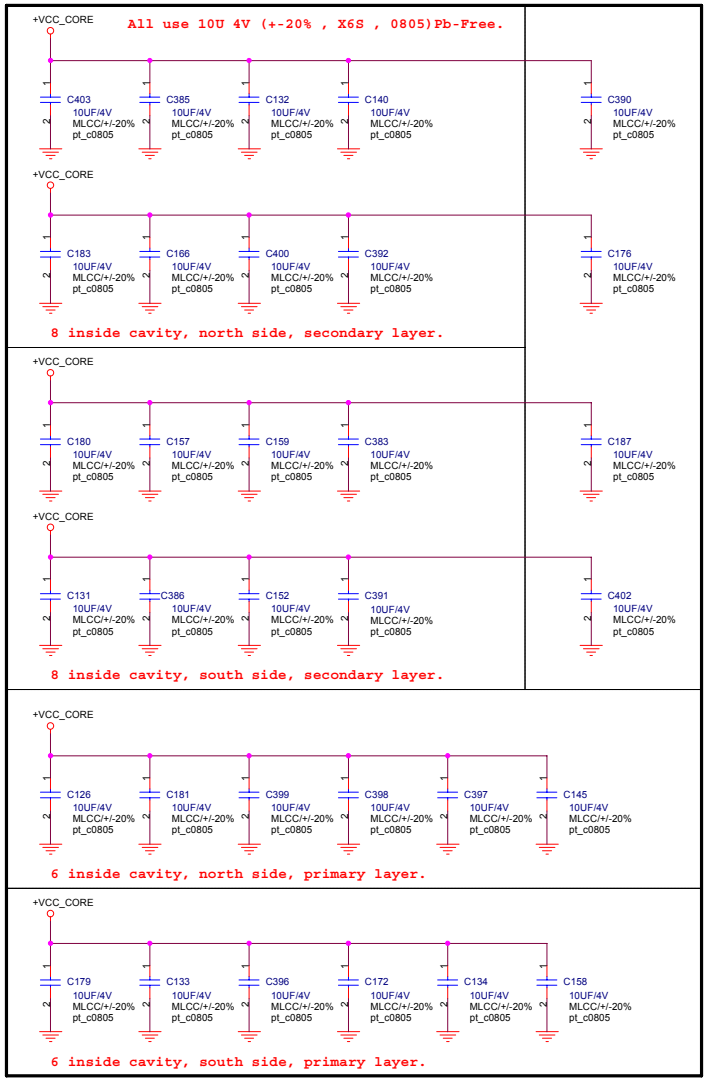


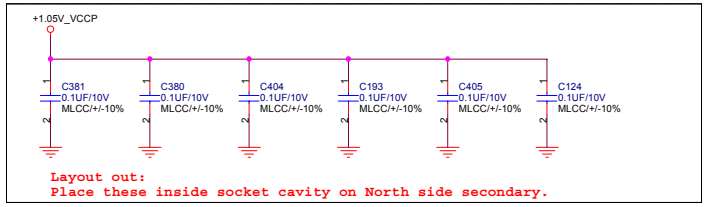
| PROJECT: Lanai | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | DESIGN ENGINEER : |
|---|---|---|---|---|---|
| | 1.2 | SHEET 6 OF 68 | Power Rail | RELEASE DATE : | |

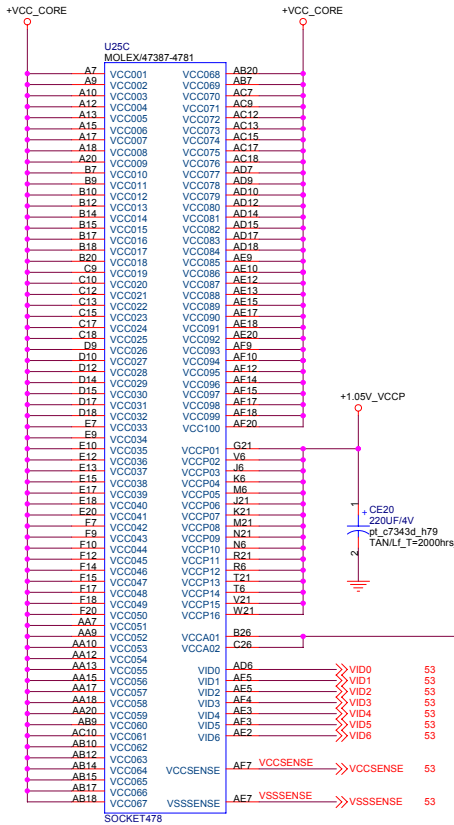


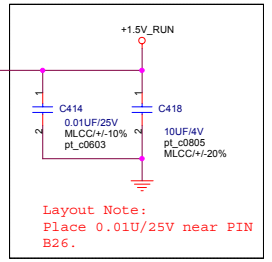

| FSB | BCLK | BSEL2 | BSEL1 | BSEL0 |
|---|---|---|---|---|
| 533 | 133 | 0 | 0 | 1 |
| 667 | 166 | 0 | 1 | 1 |
| 800 | 200 | 0 | 1 | 0 |

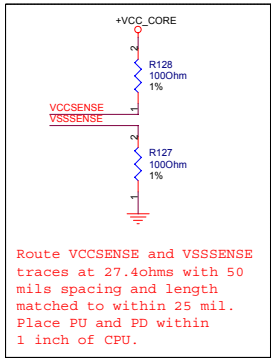
| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | 1.2 | SHEET 7 OF 68 | *MEROM CPU (1)* | RELEASE DATE : | | |

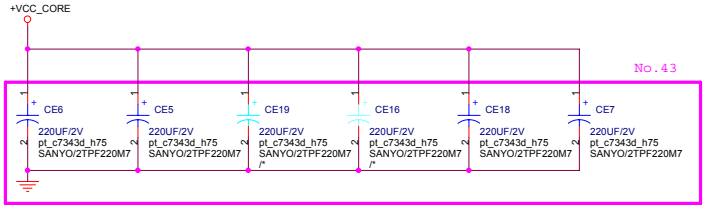


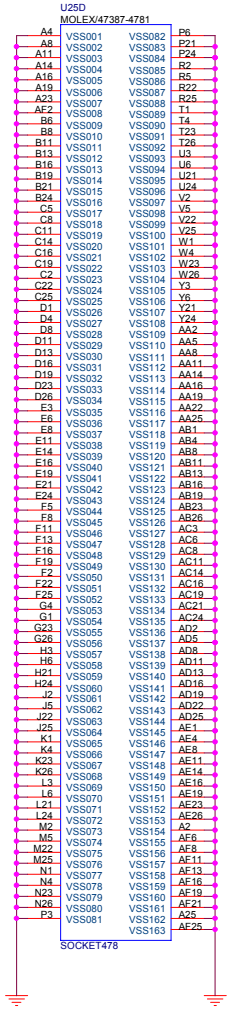



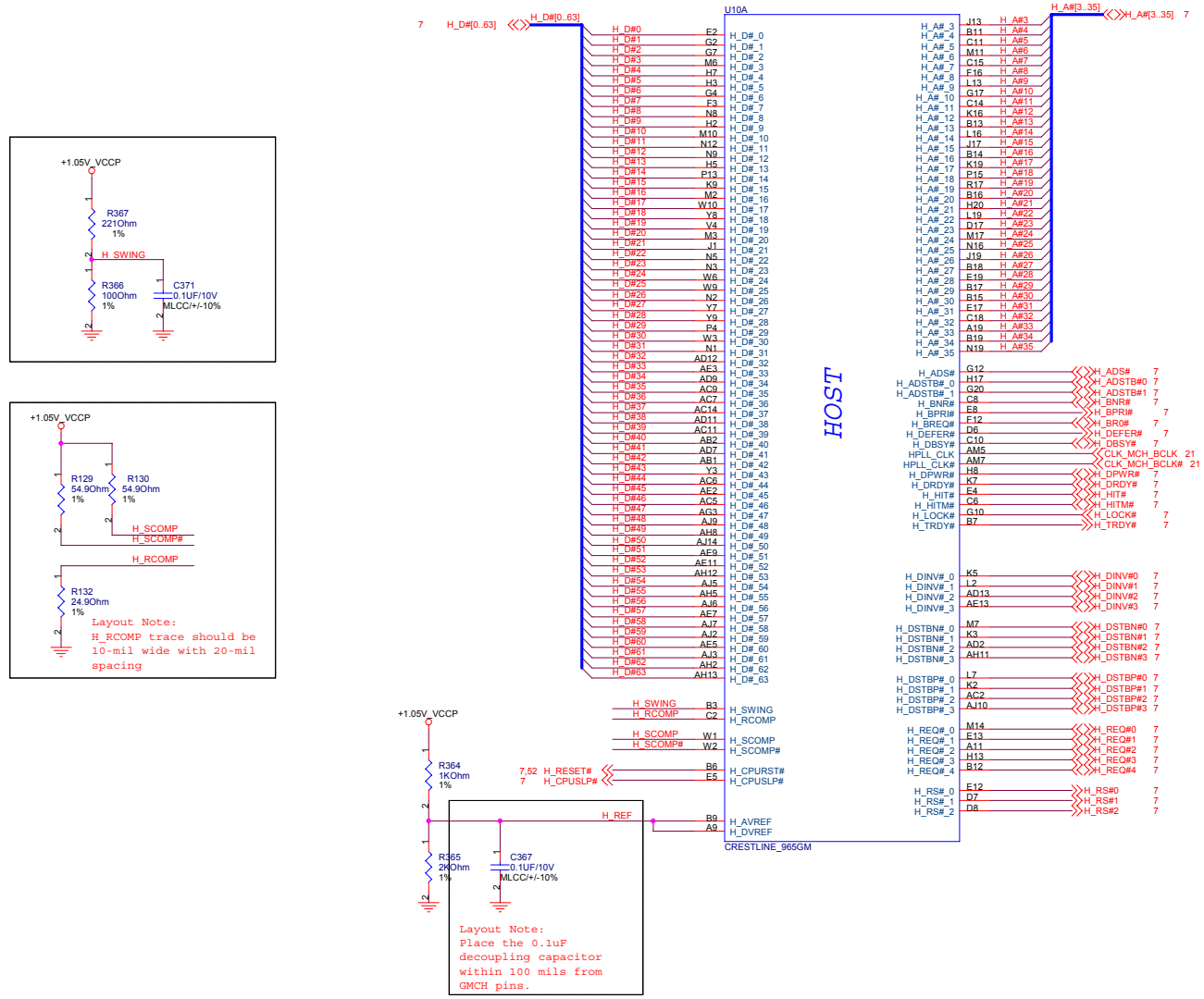




100U/25V *4 Remove to POWER CIRCUIT .




| PROJECT: Lanai | REVISION 1.2 | DATE: Monday, March 19, 2007 | DESCRIPTION: Merom CPU (2) | SCHEMATIC FILE NAME : <OrgName> | DESIGN ENGINEER : |
|---|---|---|---|---|---|
| | | SHEET 8 OF 68 | | RELEASE DATE : | |

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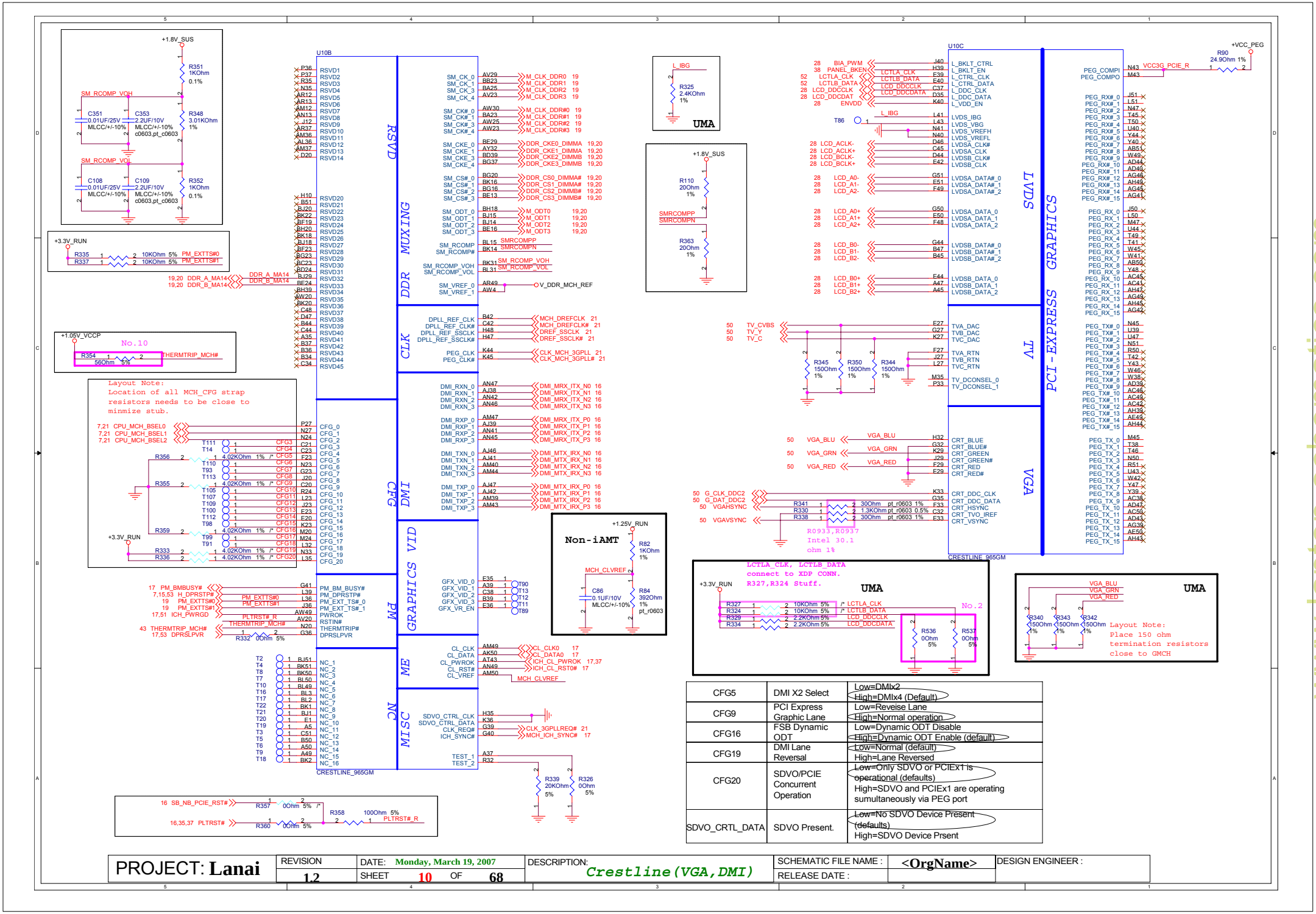
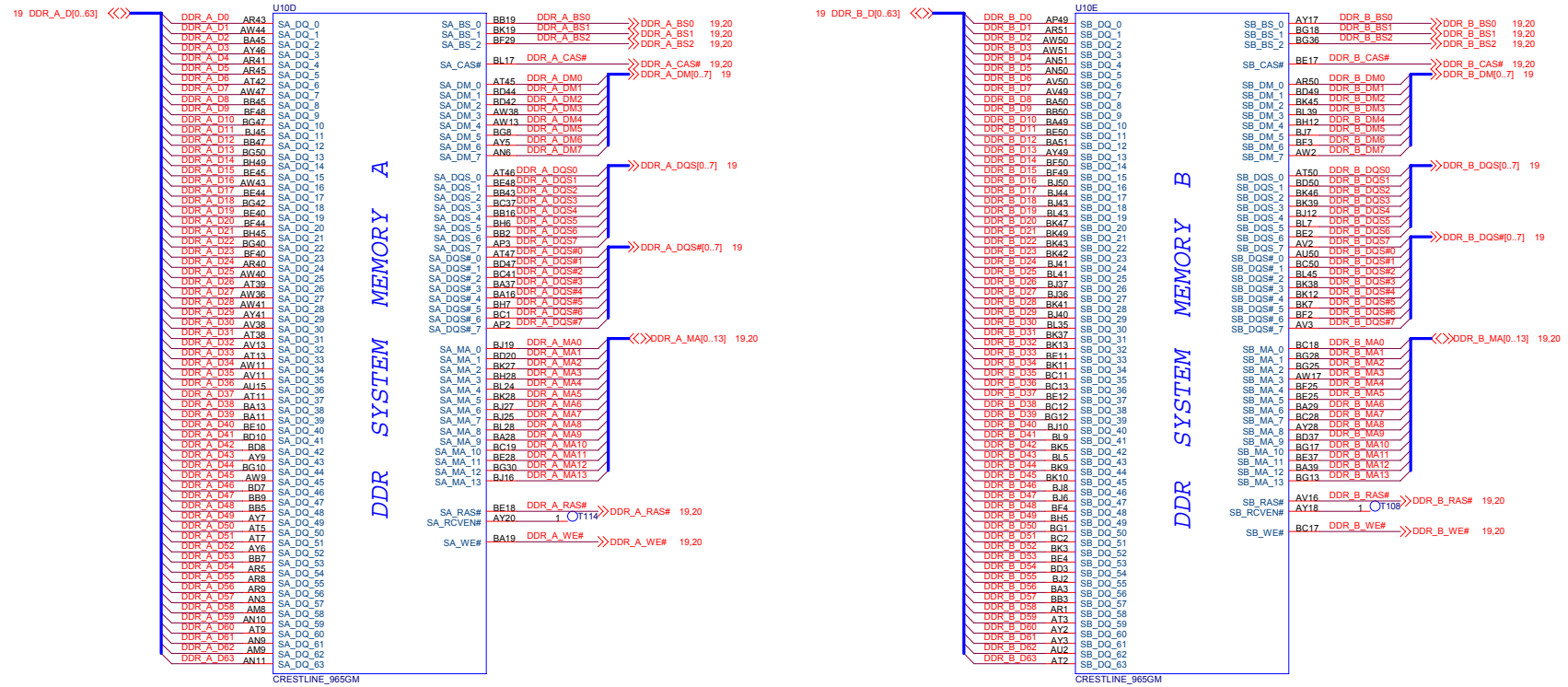
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***Crestline(HOST)*** | SCHEMATIC FILE NAME : | **<OrgName>** | DESIGN ENGINEER : |
| | | SHEET **9** OF **68** | | RELEASE DATE : | | |




| | | |
|---|---|---|
| CFG5 | DMI X2 Select | Low=DMIx2<br>High=DMIx4 (Default) |
| CFG9 | PCI Express Graphic Lane | Low=Reveise Lane<br>High=Normal operation |
| CFG16 | FSB Dynamic ODT | Low=Dynamic ODT Disable<br>High=Dynamic ODT Enable (default) |
| CFG19 | DMI Lane Reversal | Low=Normal (default)<br>High=Lane Reversed |
| CFG20 | SDVO/PCIE Concurrent Operation | Low=Only SDVO or PCIEx1 is operational (defaults)<br>High=SDVO and PCIEx1 are operating sumultaneously via PEG port |
| SDVO_CRTL_DATA | SDVO Present. | Low=No SDVO Device Present (defaults)<br>High=SDVO Device Prsent |

| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION: 1.2 | DATE: Monday, March 19, 2007 | DESCRIPTION: *Crestline(VGA,DMI)* | SCHEMATIC FILE NAME : <OrgName> | DESIGN ENGINEER : |
| | | SHEET 10 OF 68 | | RELEASE DATE : | |




| | | | | | | |
|---|---|---|---|---|---|---|
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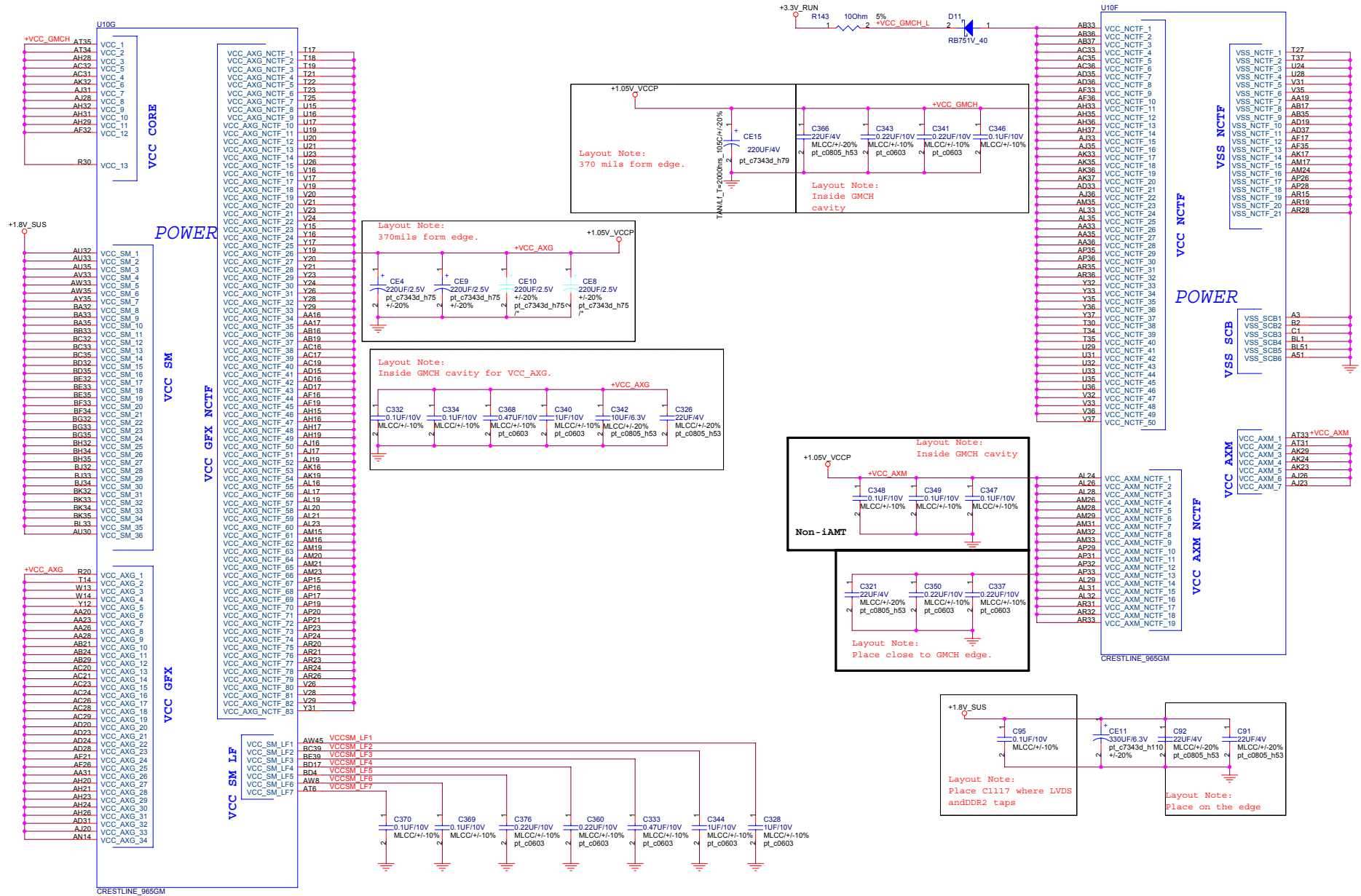
| | | SHEET **11** OF **68** | | RELEASE DATE : | | |

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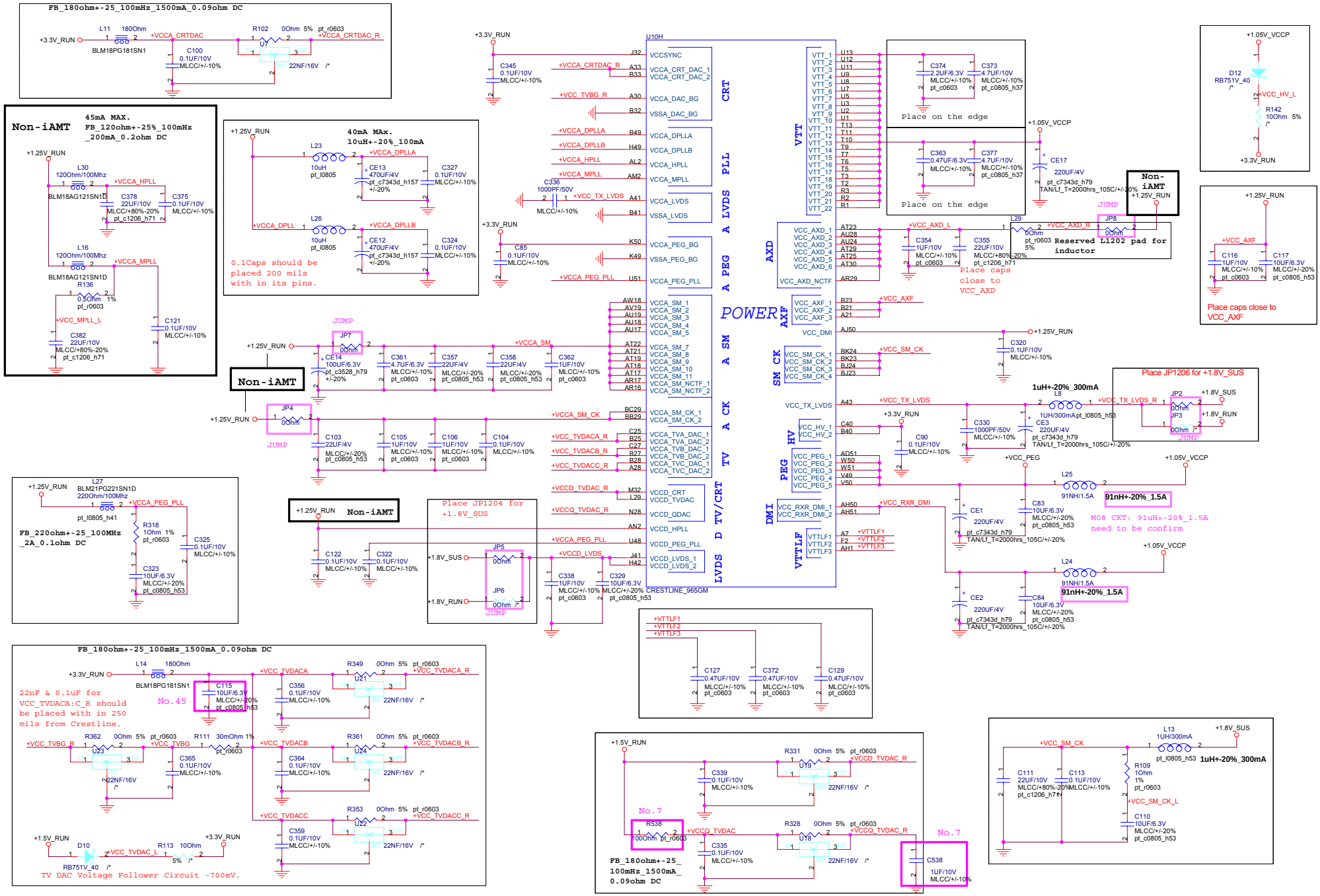
| | | SHEET 12 OF 68 | | RELEASE DATE : | |

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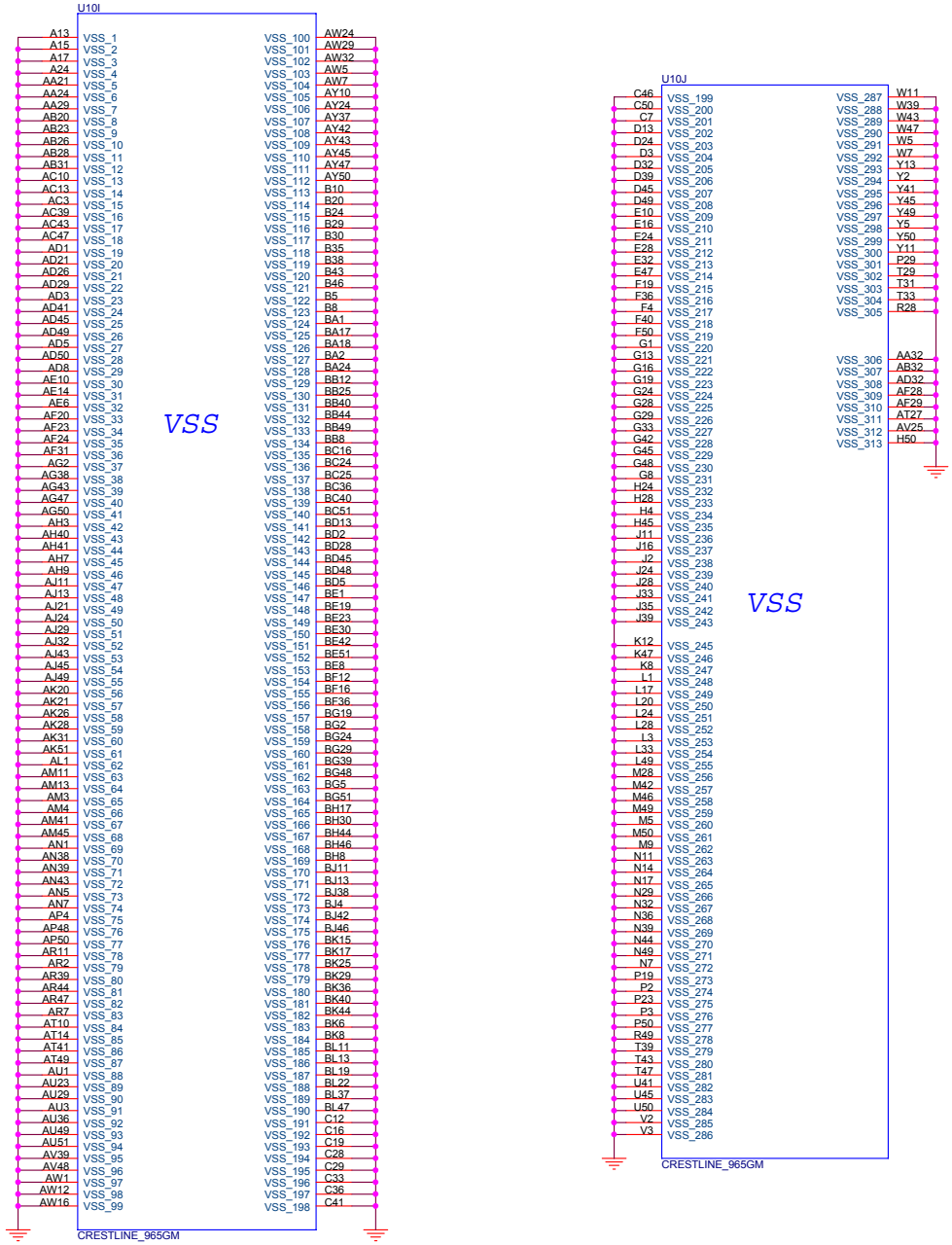
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***Crestline(POWER)*** | SCHEMATIC FILE NAME : **<OrgName>** | DESIGN ENGINEER : |
| | | SHEET **13** OF **68** | | RELEASE DATE : | |

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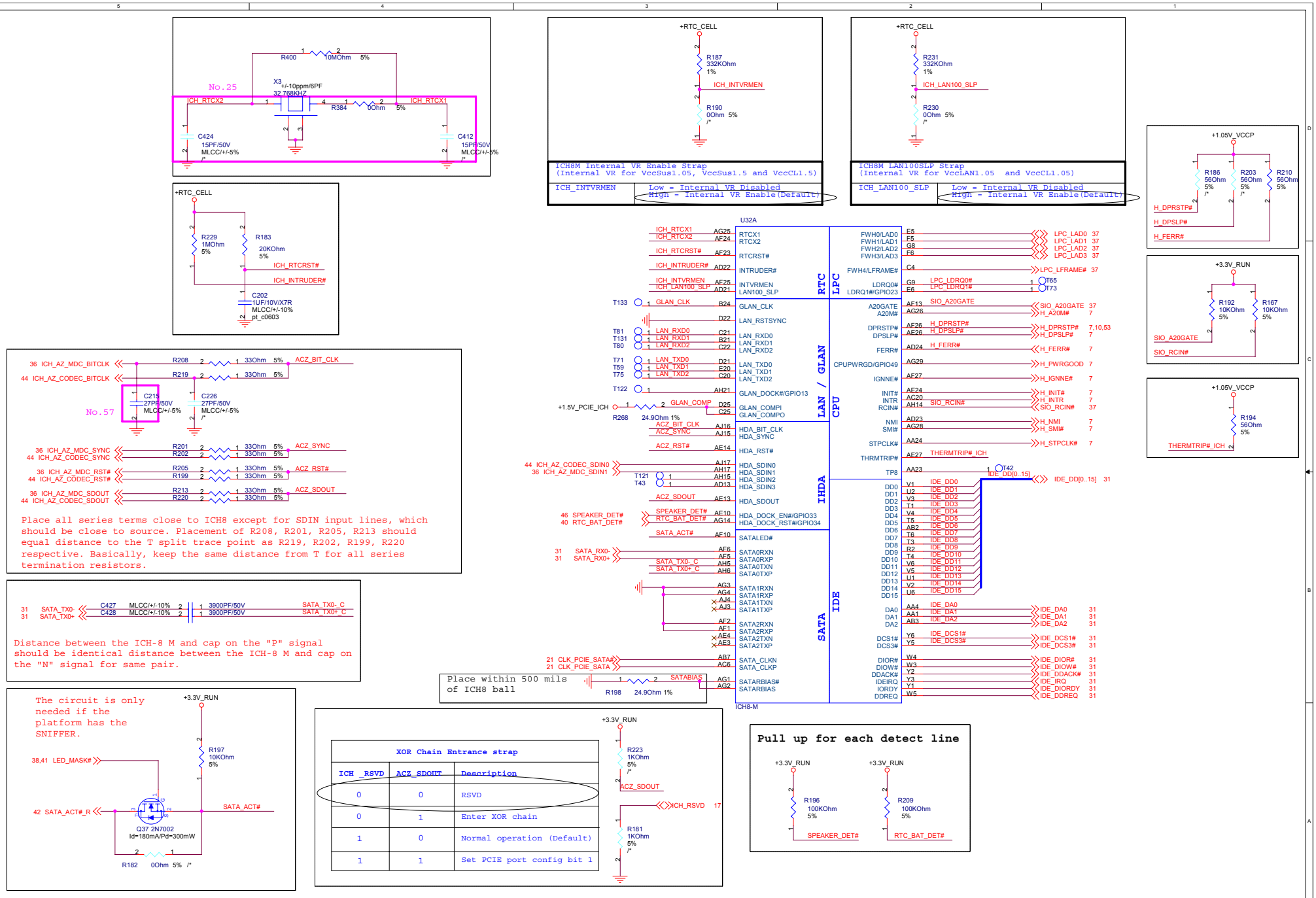
| | | SHEET 14 OF 68 | | RELEASE DATE : | |

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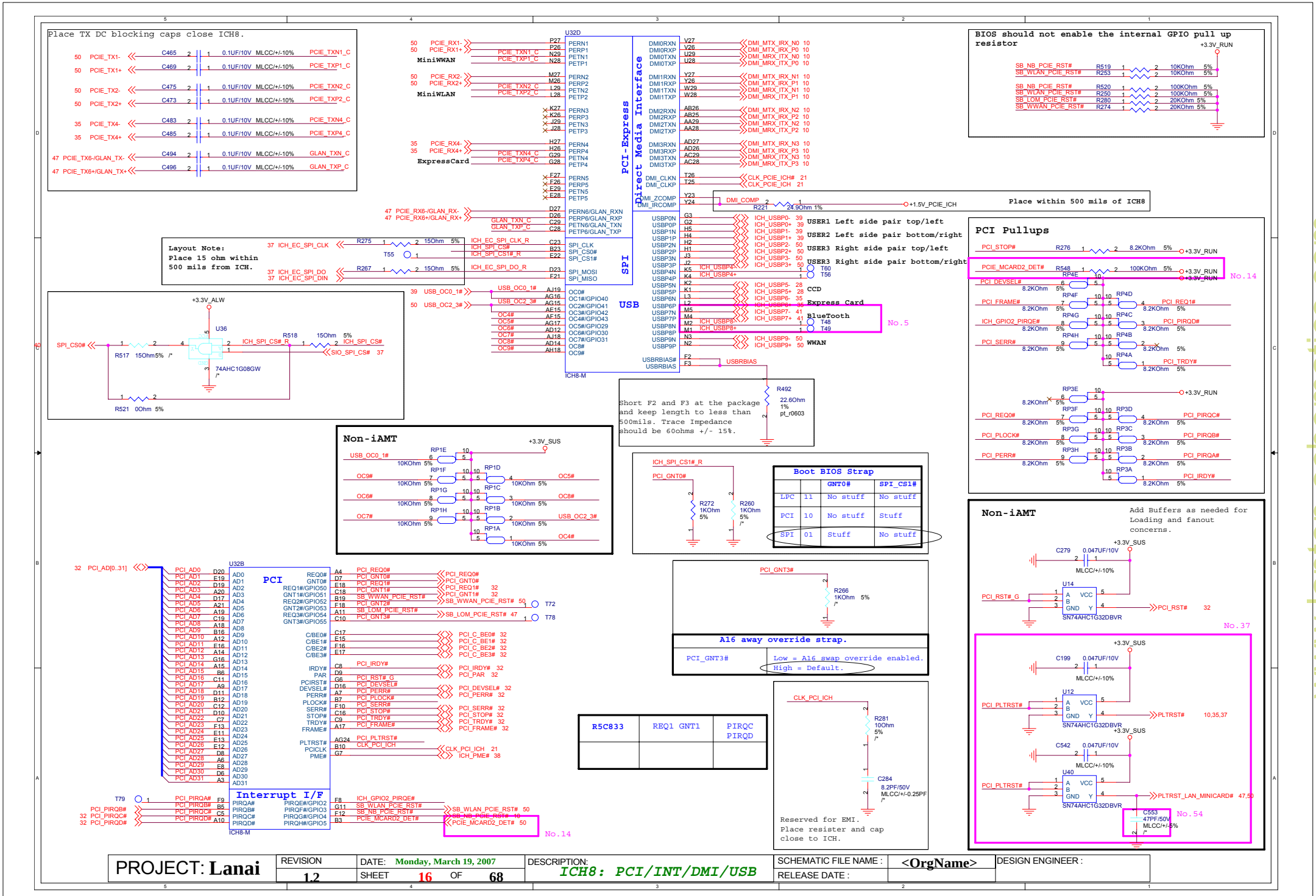
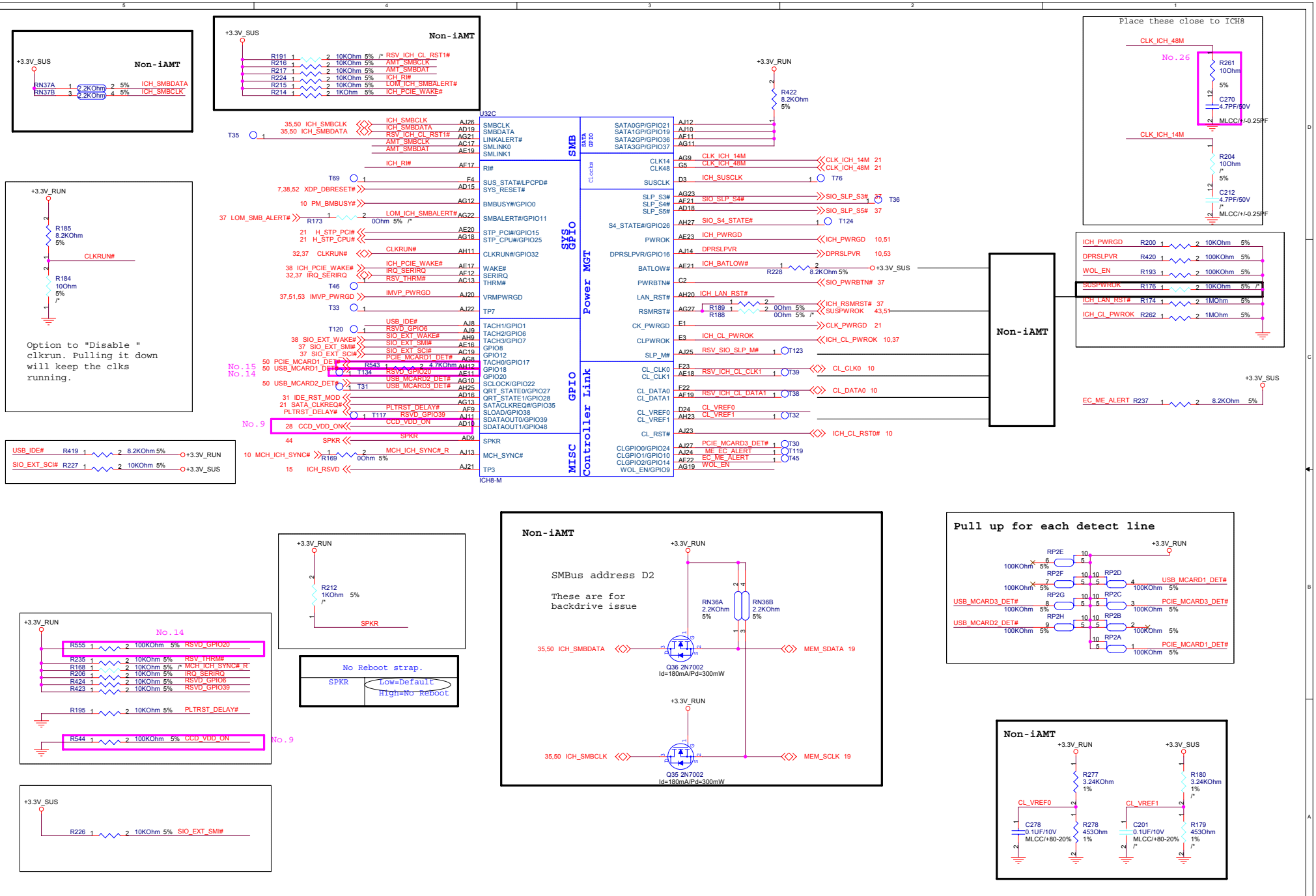
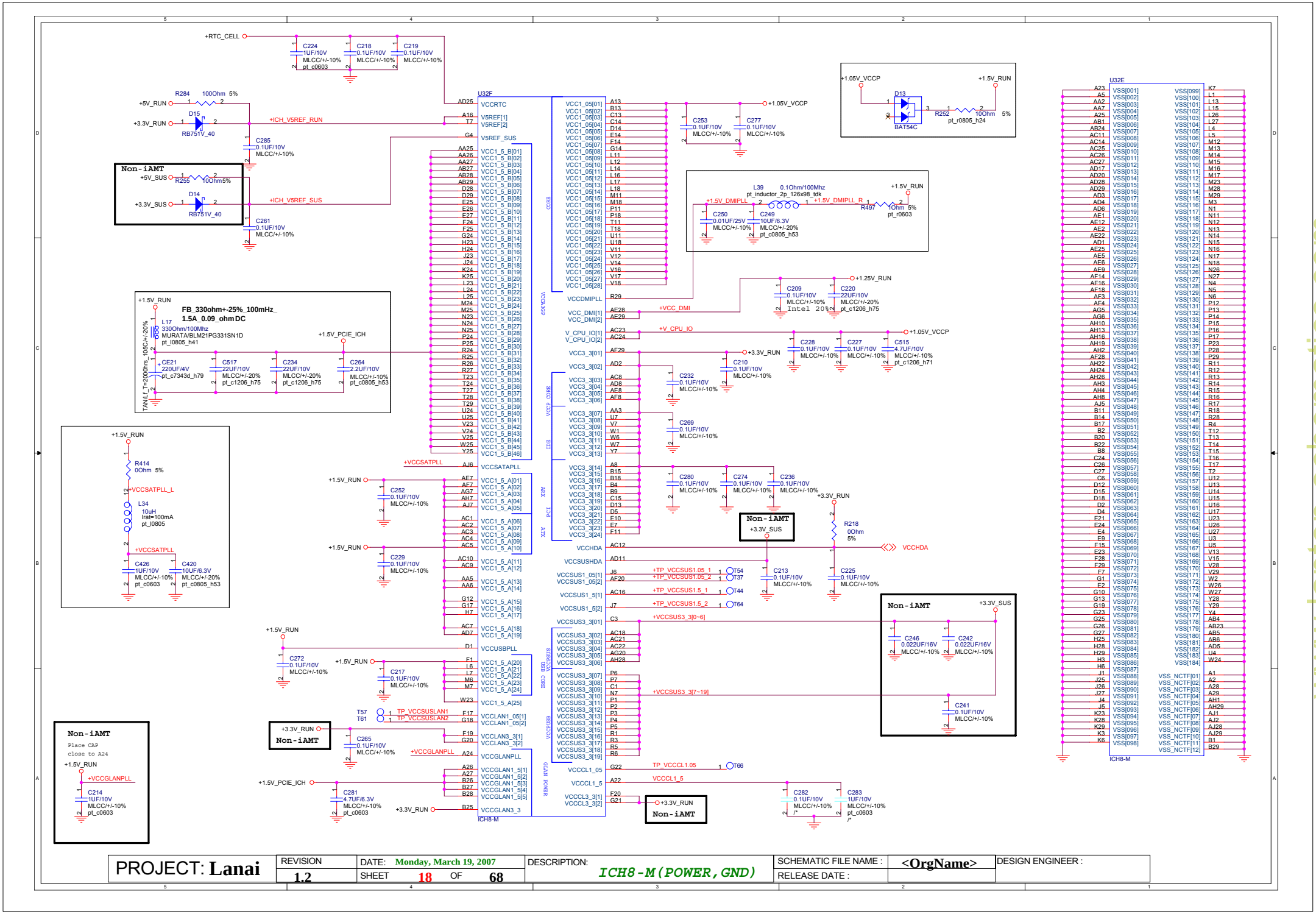
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION: 1.2 | DATE: Monday, March 19, 2007 | DESCRIPTION: *ICH8: IDE/AC97/LPC/RTC* | SCHEMATIC FILE NAME: <OrgName> | DESIGN ENGINEER: |
| | | SHEET 15 OF 68 | | RELEASE DATE: | |



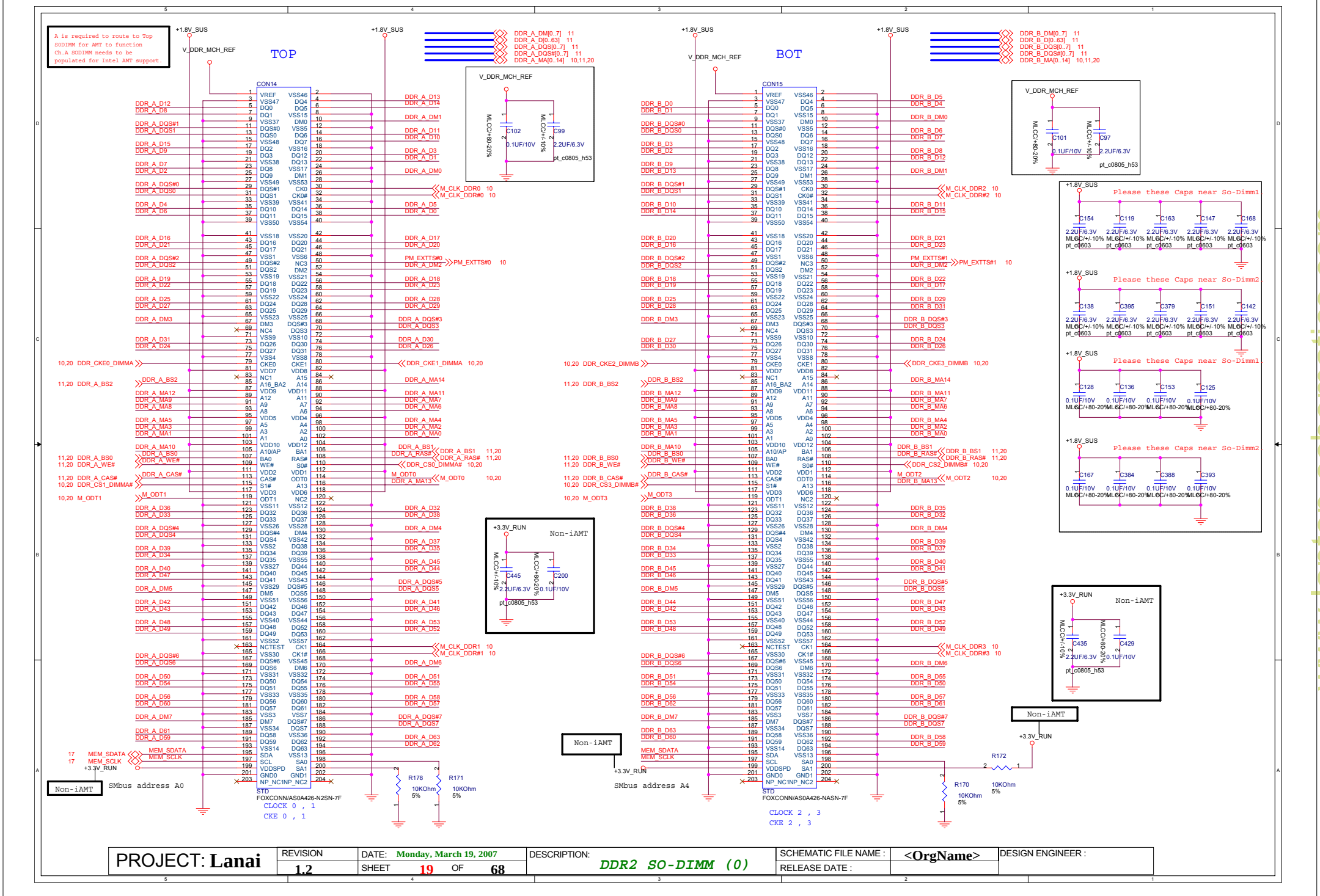

| PROJECT: Lanai | REVISION: 1.2 | DATE: Monday, March 19, 2007 | SHEET 16 OF 68 | DESCRIPTION: ICH8: PCI/INT/DMI/USB | SCHEMATIC FILE NAME: <OrgName> | RELEASE DATE: | DESIGN ENGINEER: |
|---|---|---|---|---|---|---|---|

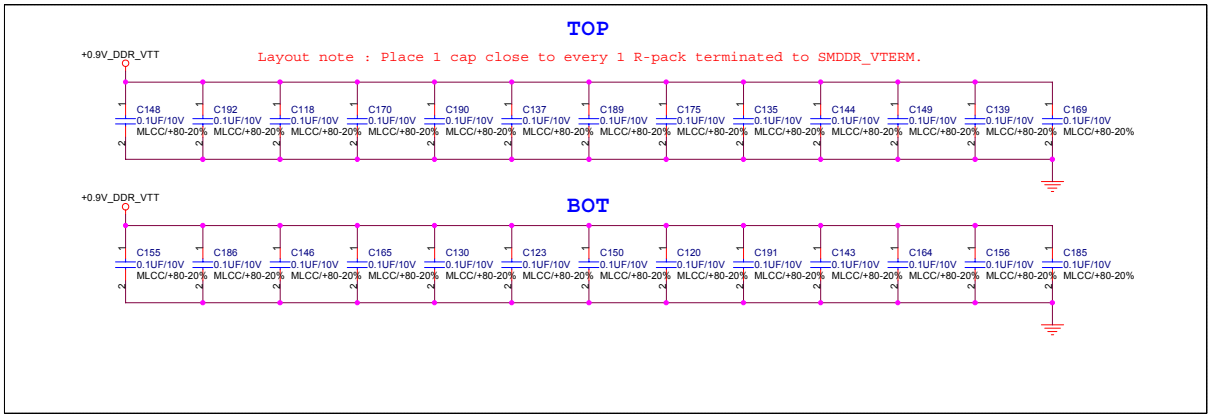


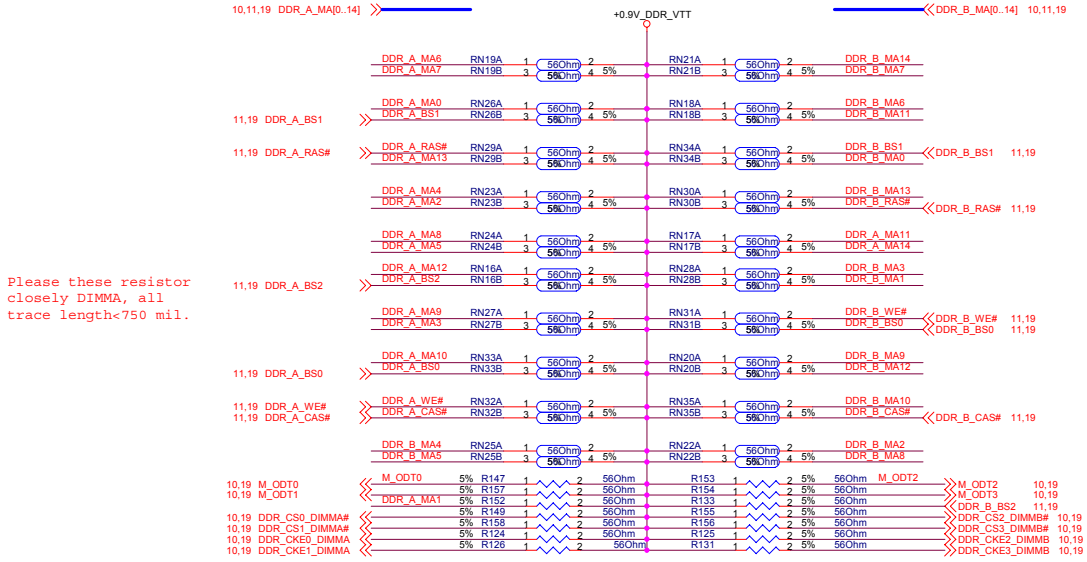

| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***ICH8: SMB/PWR/CLK/GPIO*** | SCHEMATIC FILE NAME : **<OrgName>** | DESIGN ENGINEER : |
| | | SHEET **17** OF **68** | | RELEASE DATE : | |




| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION: **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: *ICH8-M(POWER,GND)* | SCHEMATIC FILE NAME: <OrgName> | DESIGN ENGINEER: |
| | | SHEET 18 OF 68 | | RELEASE DATE: | |



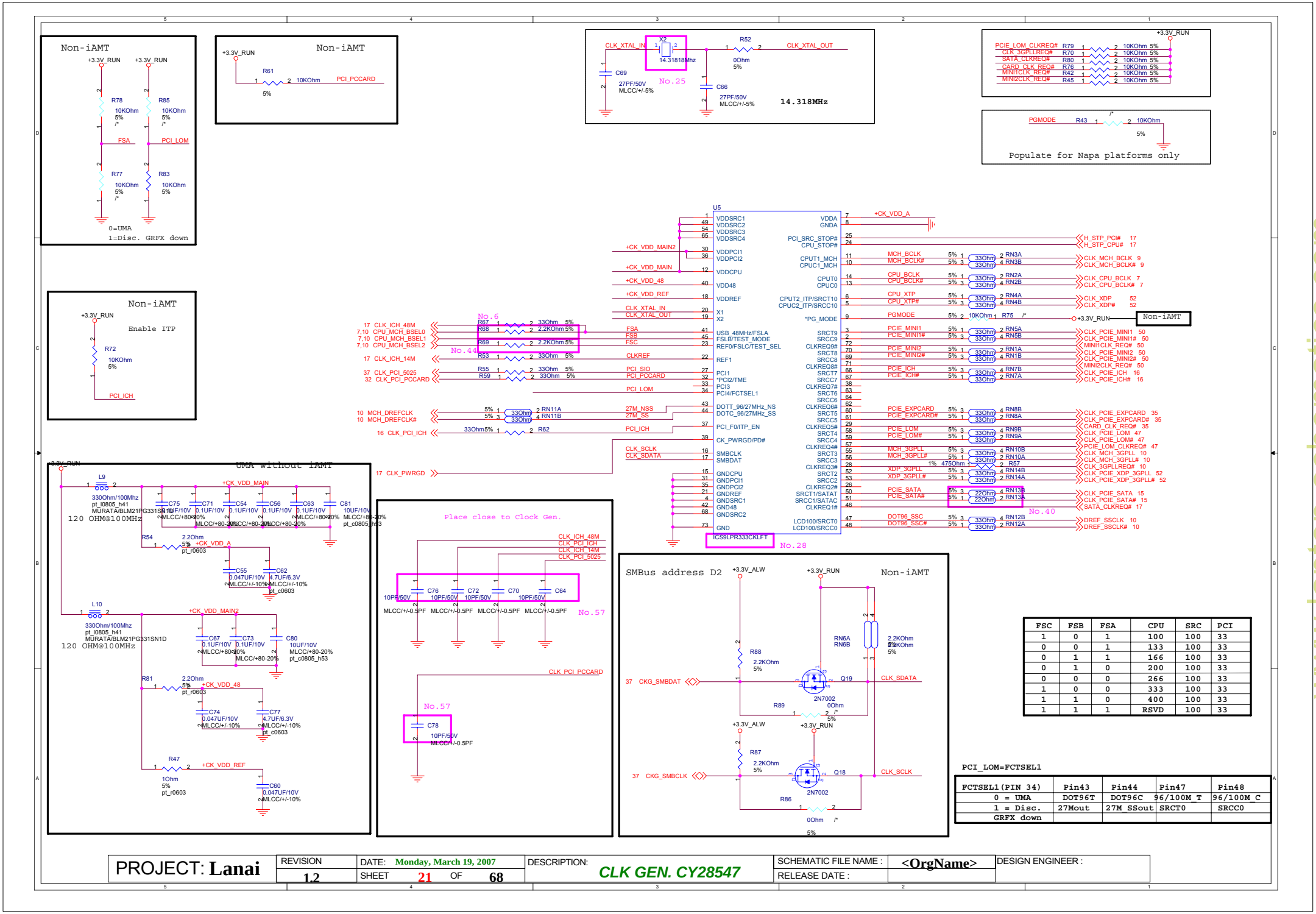



Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | 1.2 | SHEET 20 OF 68 | *DDR2 SO-DIMM (1)* | RELEASE DATE : | | |



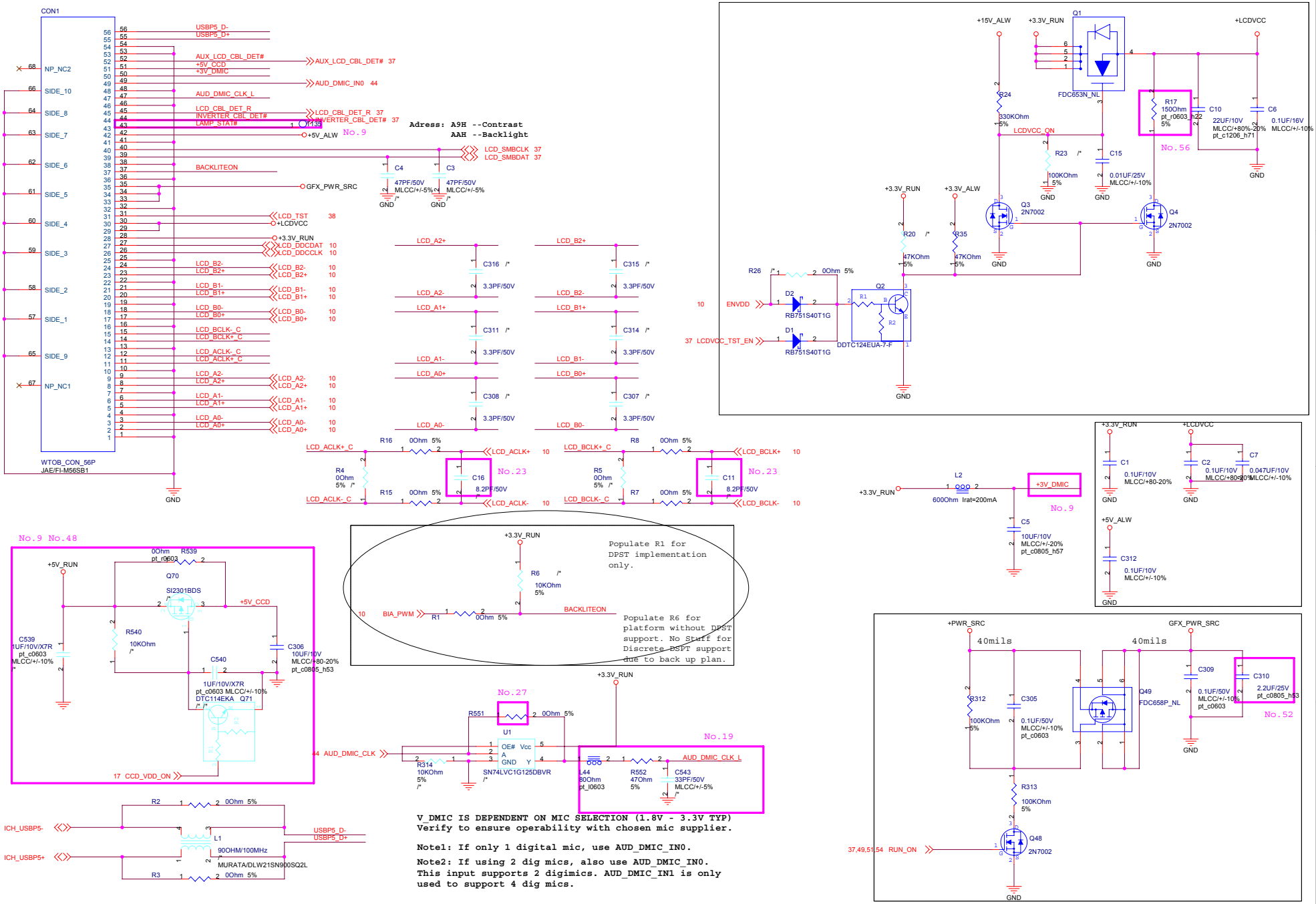
| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | 1.2 | SHEET 23 OF 68 | | RELEASE DATE : | | |

| PROJECT: **Lanai** | REVISION | DATE: **Monday, March 19, 2007** | DESCRIPTION: | SCHEMATIC FILE NAME : | **<OrgName>** | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | **1.2** | SHEET **24** OF **68** | | RELEASE DATE : | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
| | 1.2 | SHEET 25 OF 68 | | RELEASE DATE : | | |

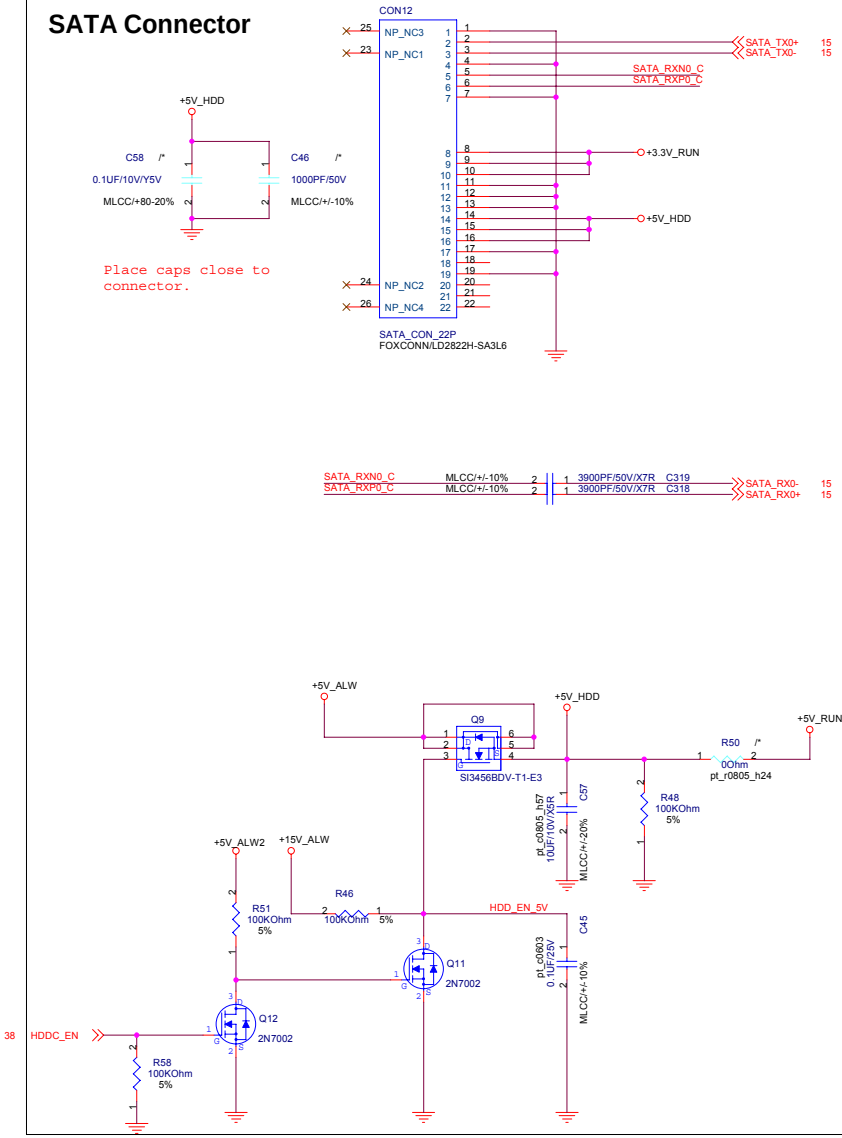
| PROJECT: **Lanai** | REVISION | DATE: **Monday, March 19, 2007** | DESCRIPTION: | SCHEMATIC FILE NAME : | | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | **1.2** | SHEET **26** OF **68** | | RELEASE DATE : | | |

| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: | SCHEMATIC FILE NAME : | DESIGN ENGINEER : **Sean Kuo** |
| | | SHEET **27** OF **68** | | RELEASE DATE : | |

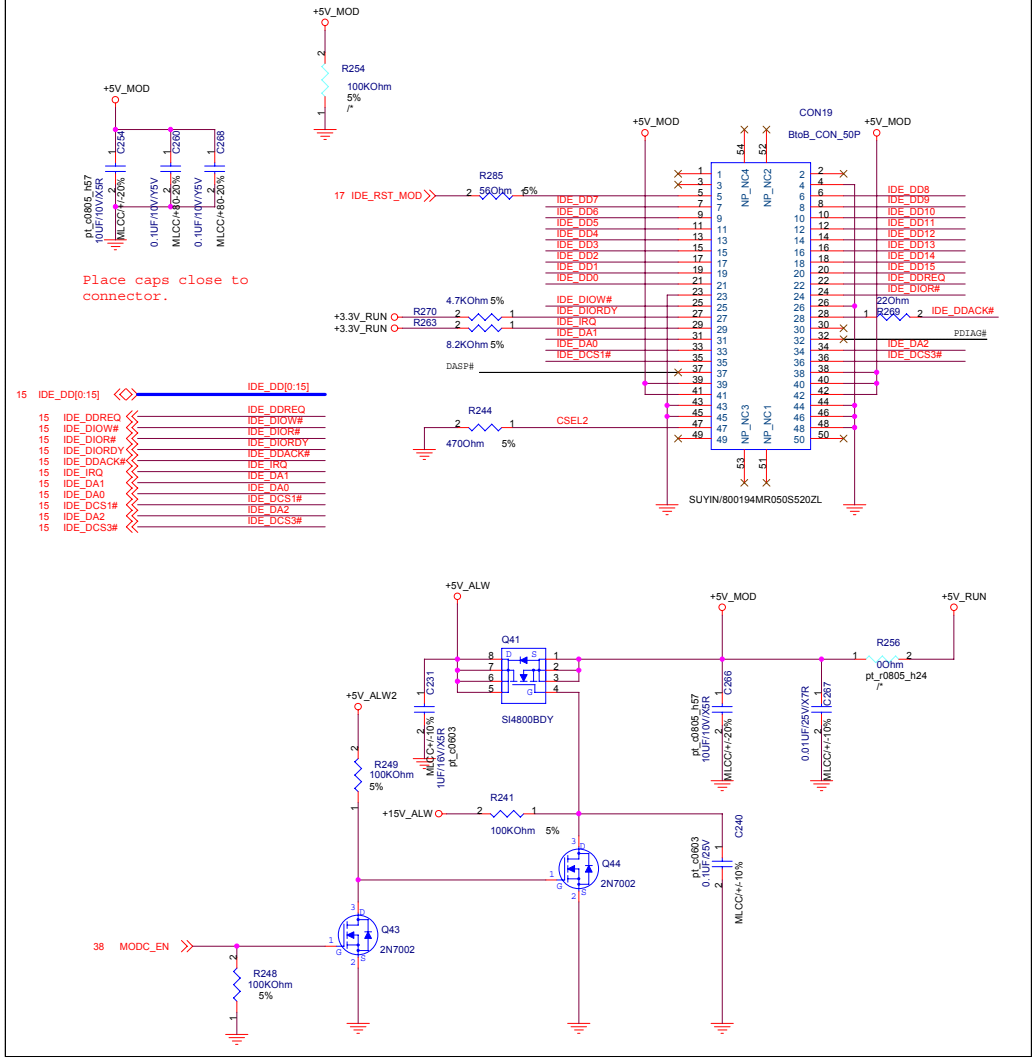



| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | | DESIGN ENGINEER : |
| | 1.2 | SHEET 28 OF 68 | *LVDS CON* | RELEASE DATE : | | |

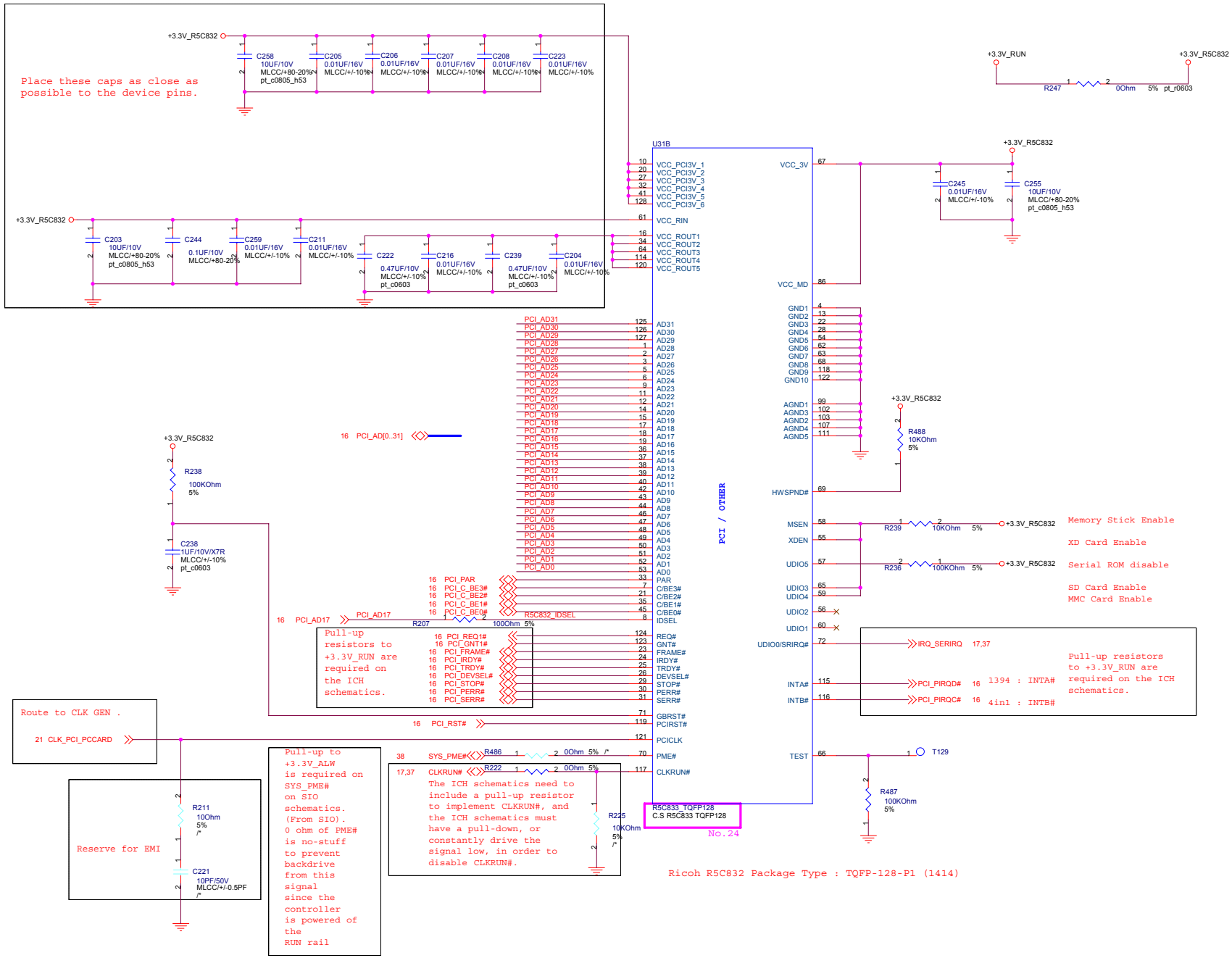
## SATA Connector



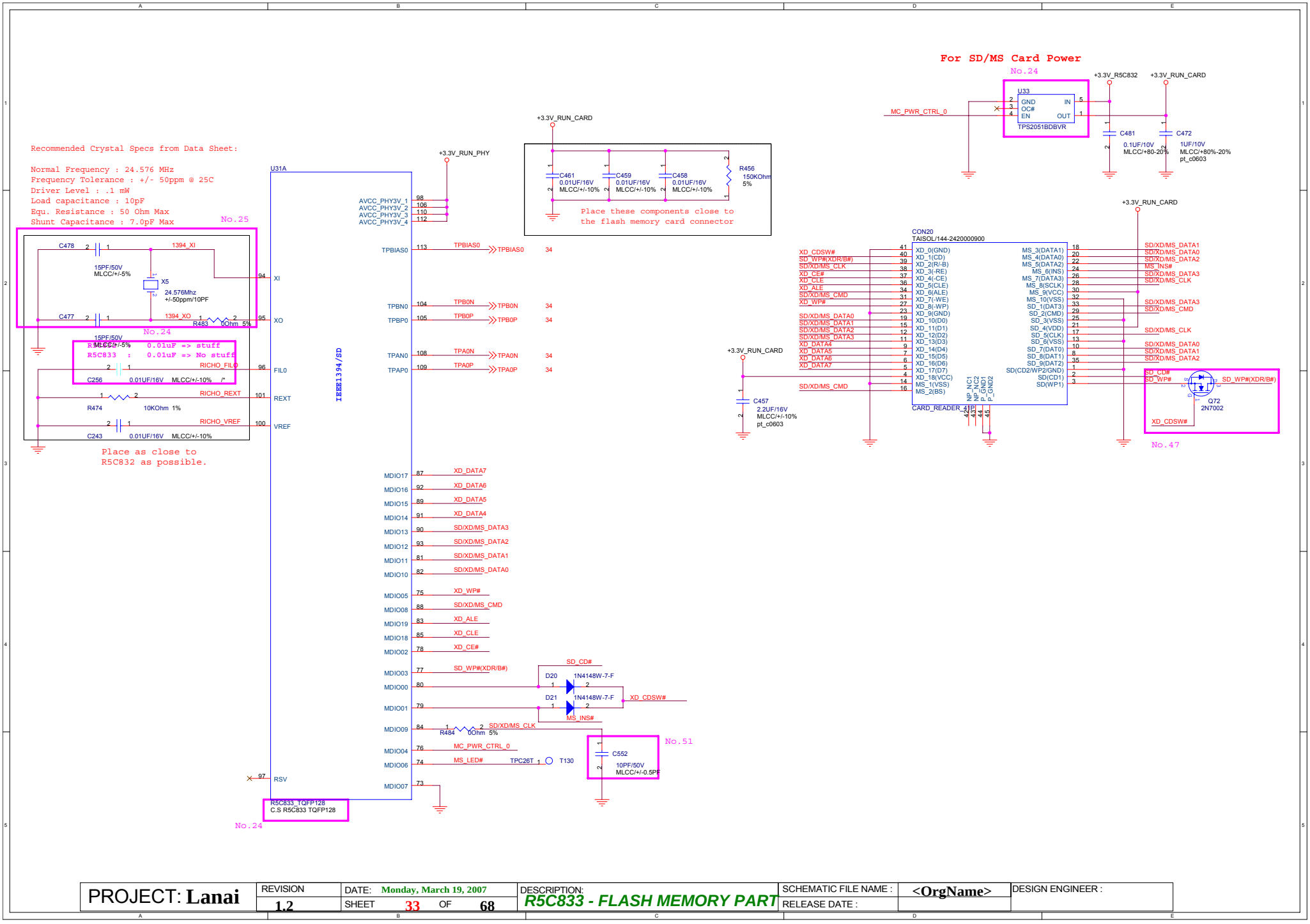

## ODD Connector



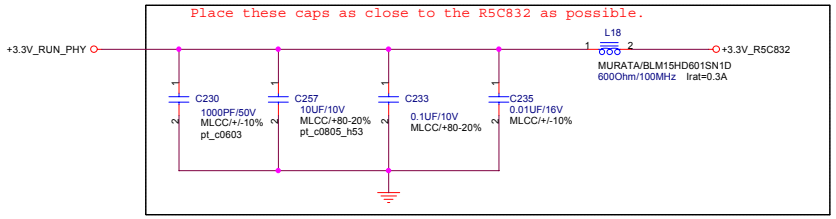

| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: *SATA (HDD & CD_ROM)* | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
| | | SHEET 31 OF 68 | | RELEASE DATE : | | |

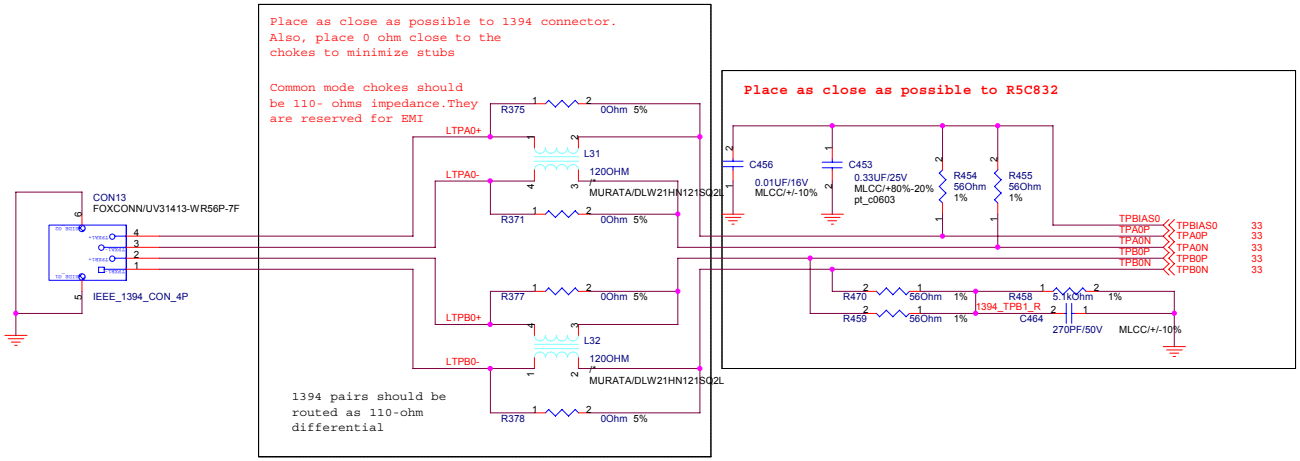



| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***R5C833 - PCI INTERFACE*** | SCHEMATIC FILE NAME : **<OrgName>** | DESIGN ENGINEER : |
| | | SHEET **32** OF **68** | | RELEASE DATE : | |



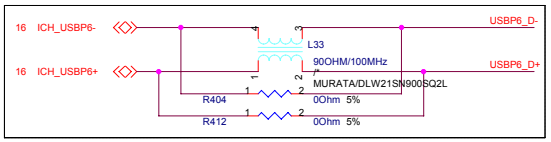

| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: ***R5C833 - FLASH MEMORY PART*** | SCHEMATIC FILE NAME : | **<OrgName>** | DESIGN ENGINEER : |
| | | SHEET **33** OF **68** | | RELEASE DATE : | | |

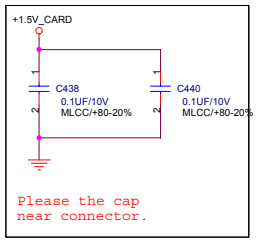


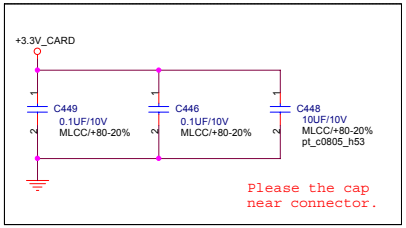



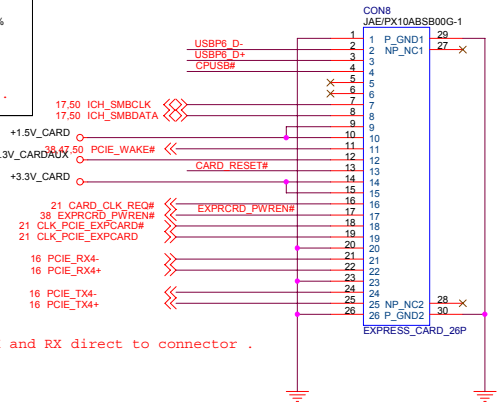

| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: *R5C833 - IEEE1394 PART* | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
| | | SHEET 34 OF 68 | | RELEASE DATE : | | |

# Express Card



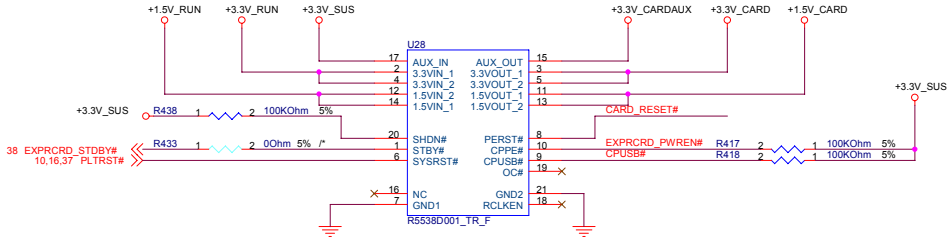



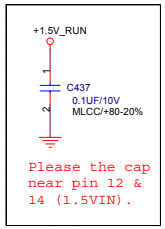



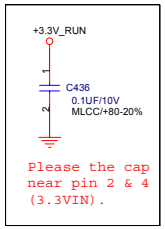



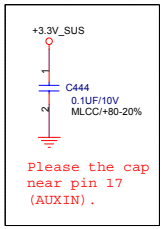

PCI-Express TX and RX direct to connector .

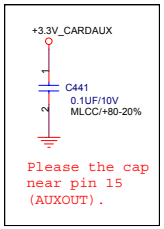
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

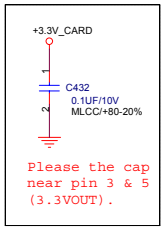


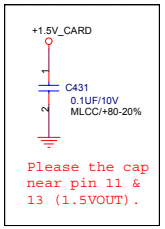



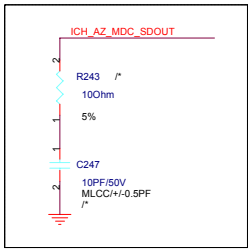



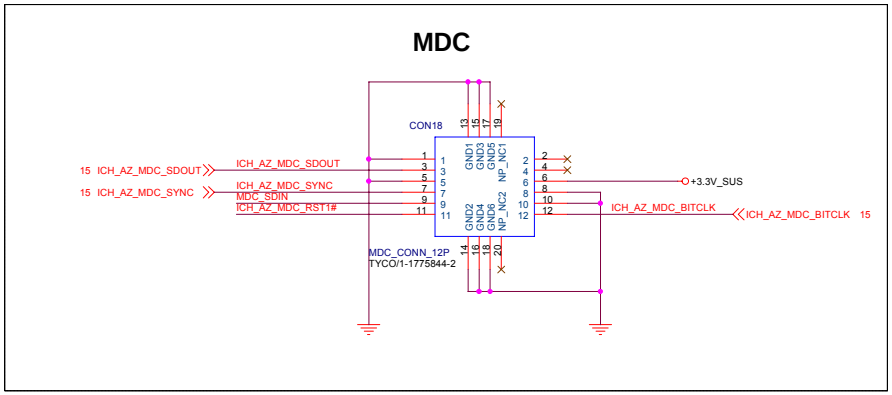



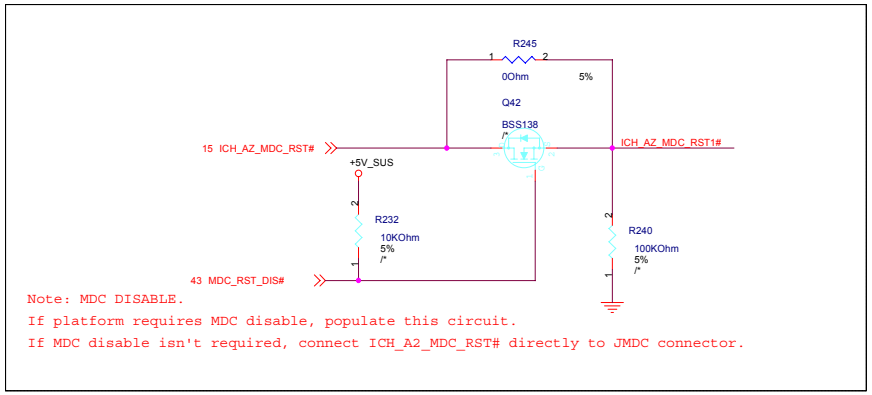



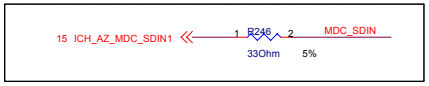



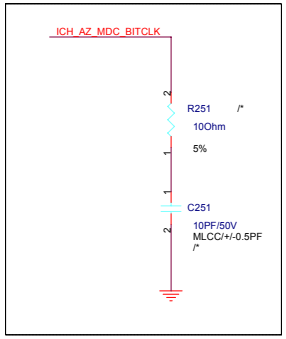

| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | 1.2 | SHEET 35 OF 68 | *PCI-Express Card* | RELEASE DATE : | | *Terry_Lin* |

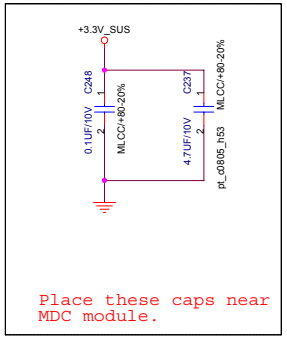
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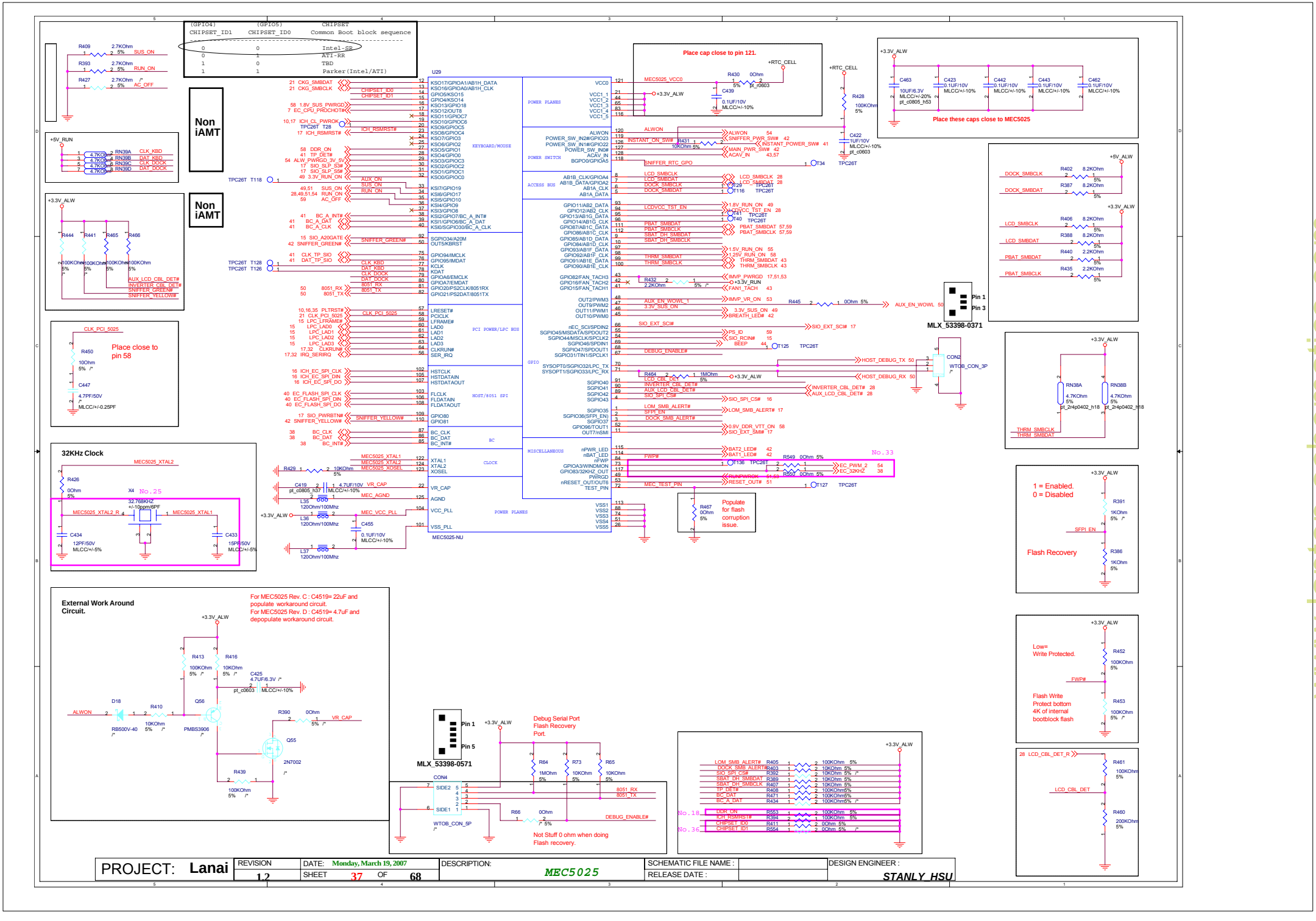
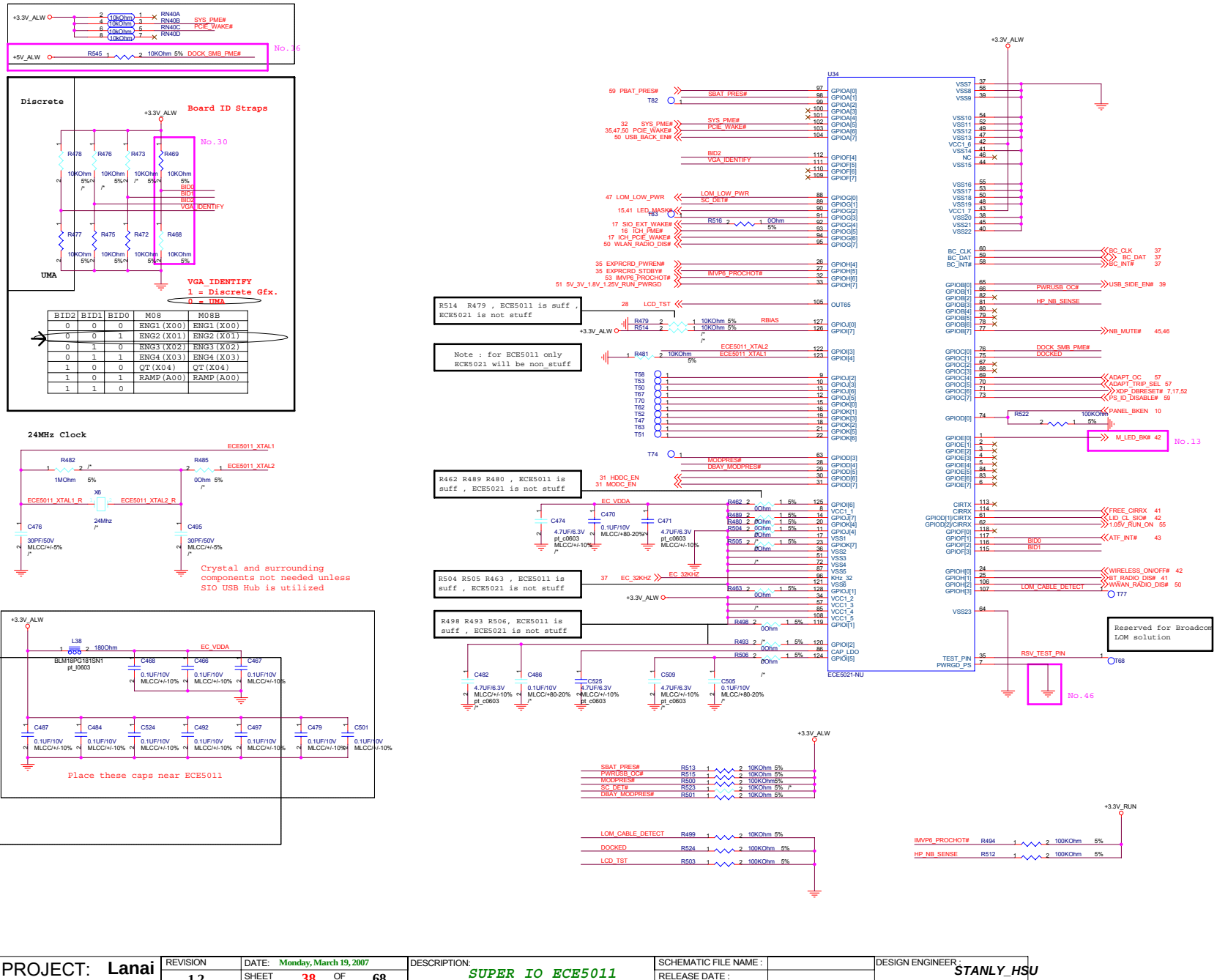
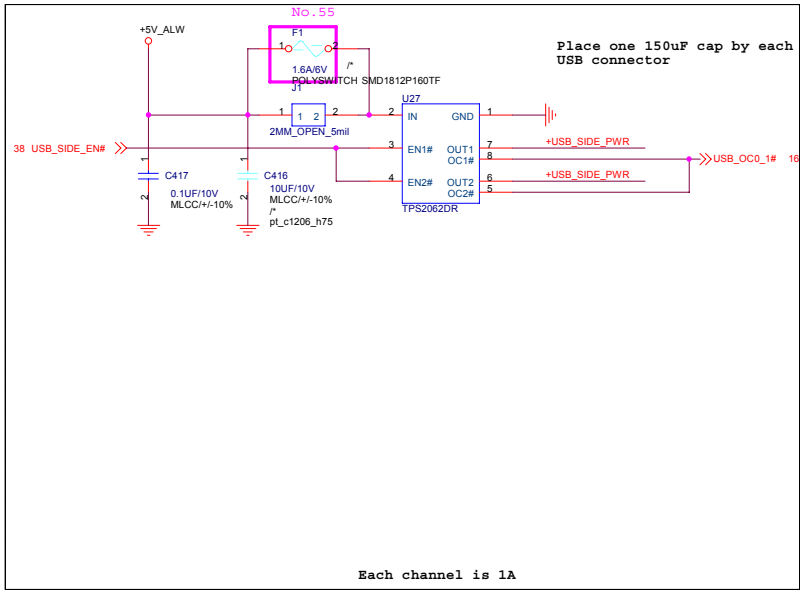
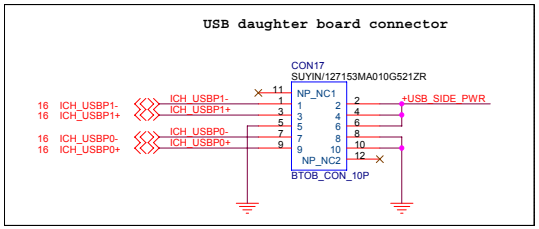
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***MDC CONN*** | SCHEMATIC FILE NAME : **<OrgName>** | DESIGN ENGINEER : |
| | | SHEET **36** OF **68** | | RELEASE DATE : | |






| PROJECT: Lanai | REVISION 1.2 | DATE: Monday, March 19, 2007 | SHEET 38 OF 68 | DESCRIPTION: SUPER IO ECE5011 | SCHEMATIC FILE NAME : | RELEASE DATE : | DESIGN ENGINEER : STANLY_HSU |
|---|---|---|---|---|---|---|---|

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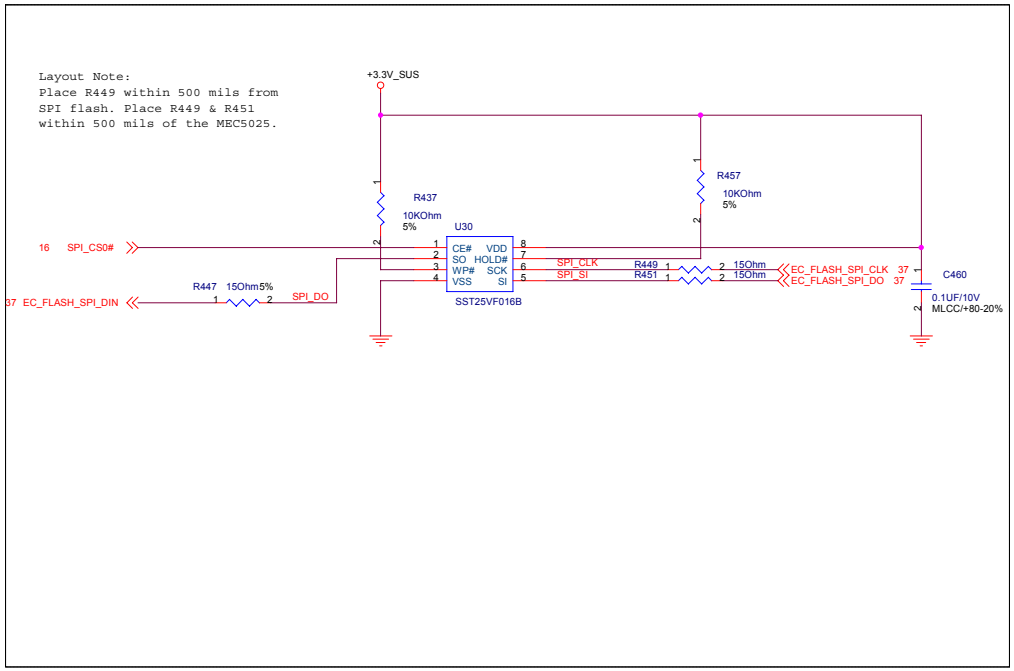
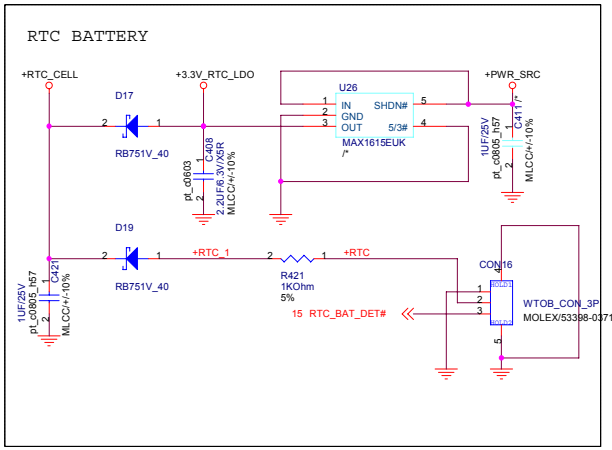
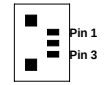
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: ***USB PORT x 2*** | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : ***Terry_Lin*** |
| | | SHEET 39 OF 68 | | RELEASE DATE : | | |




MLX_53398-0371

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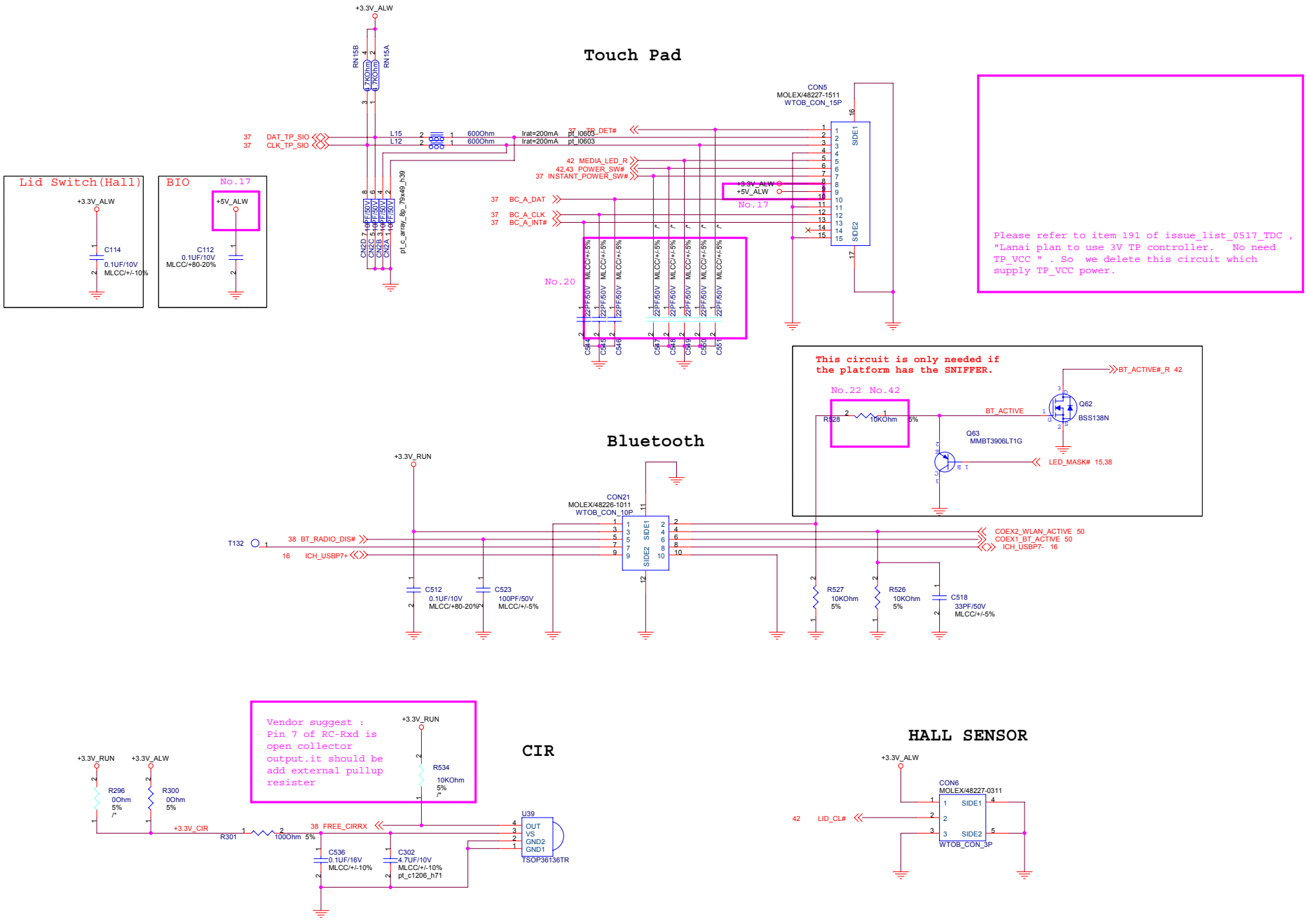
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***FLASH & RTC*** | SCHEMATIC FILE NAME : | **<OrgName>** | DESIGN ENGINEER : ***C.L. Ho*** |
| | | SHEET **40** OF **68** | | RELEASE DATE : | | |

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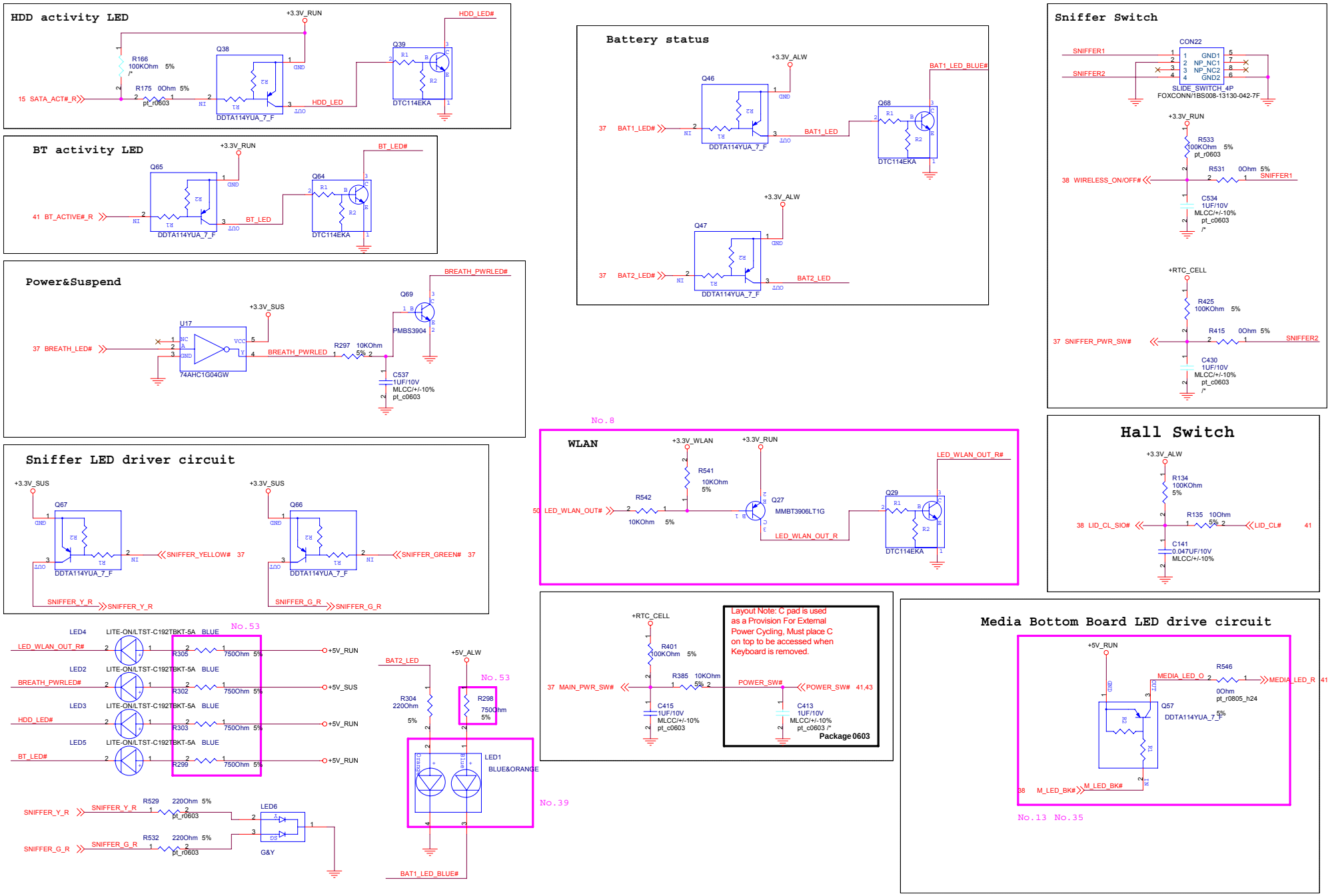
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: **TOUCH PAD & BT & CIR & LID** | SCHEMATIC FILE NAME : | **<OrgName>** | DESIGN ENGINEER : |
| | | SHEET **41** OF **68** | | RELEASE DATE : | | |

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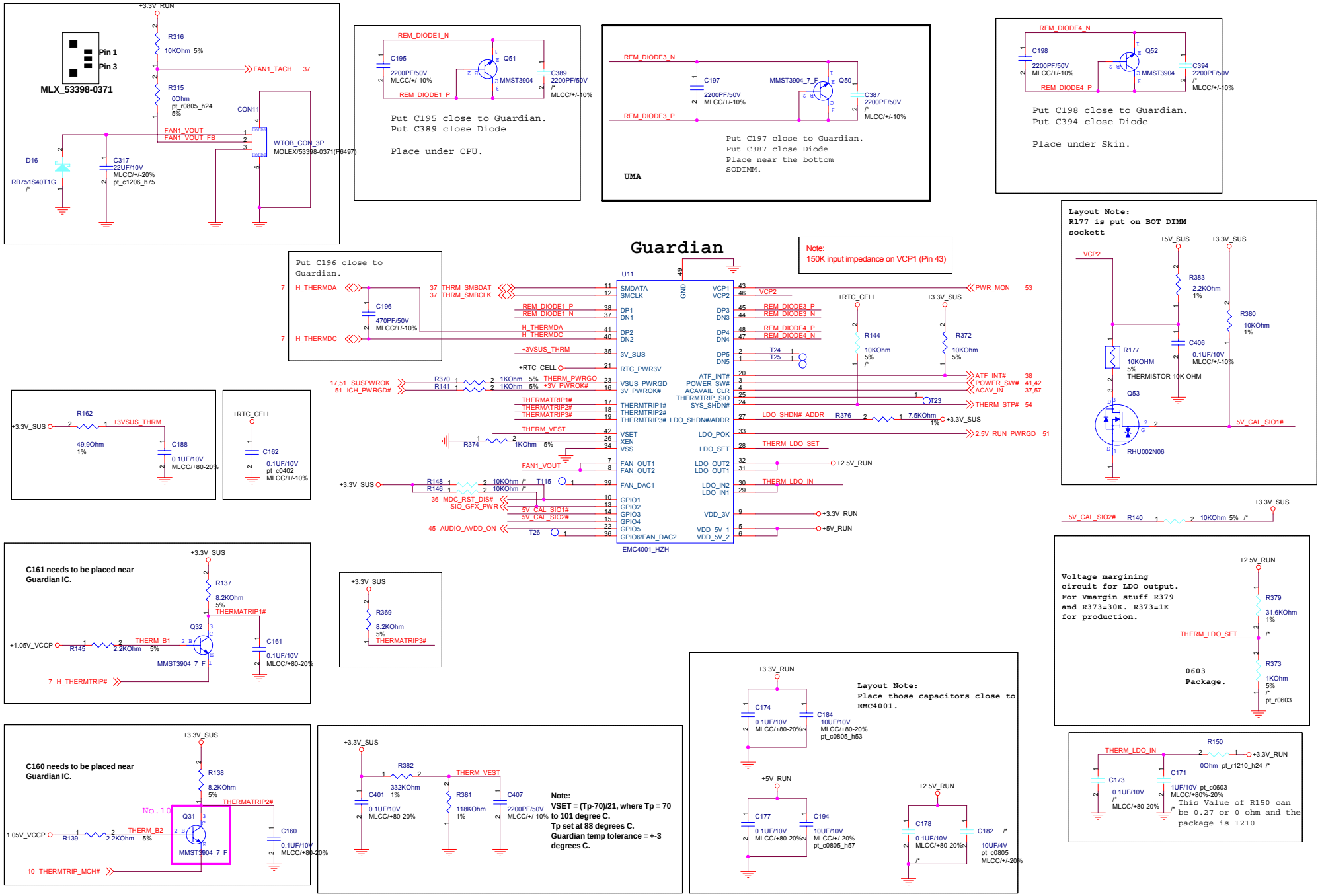
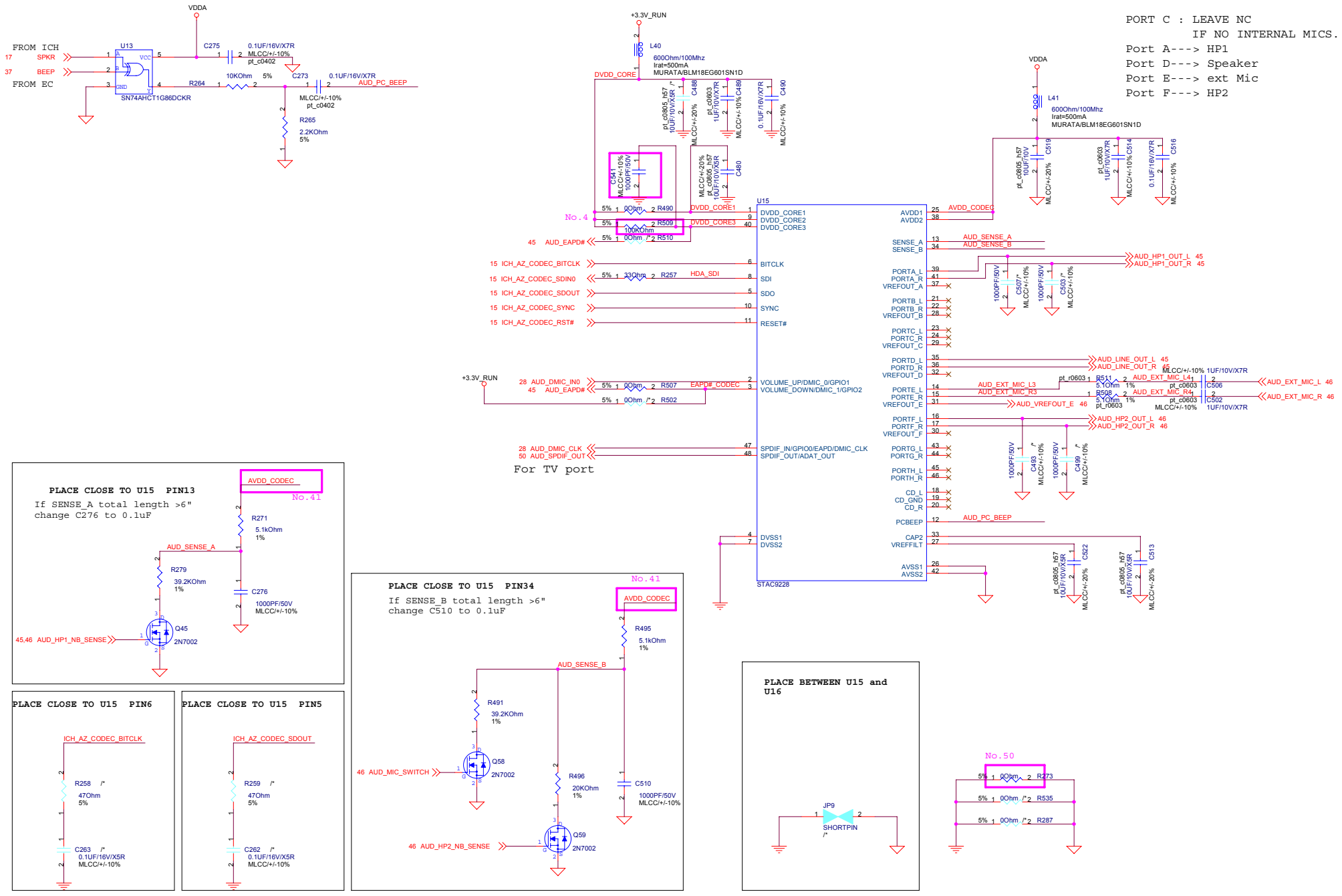
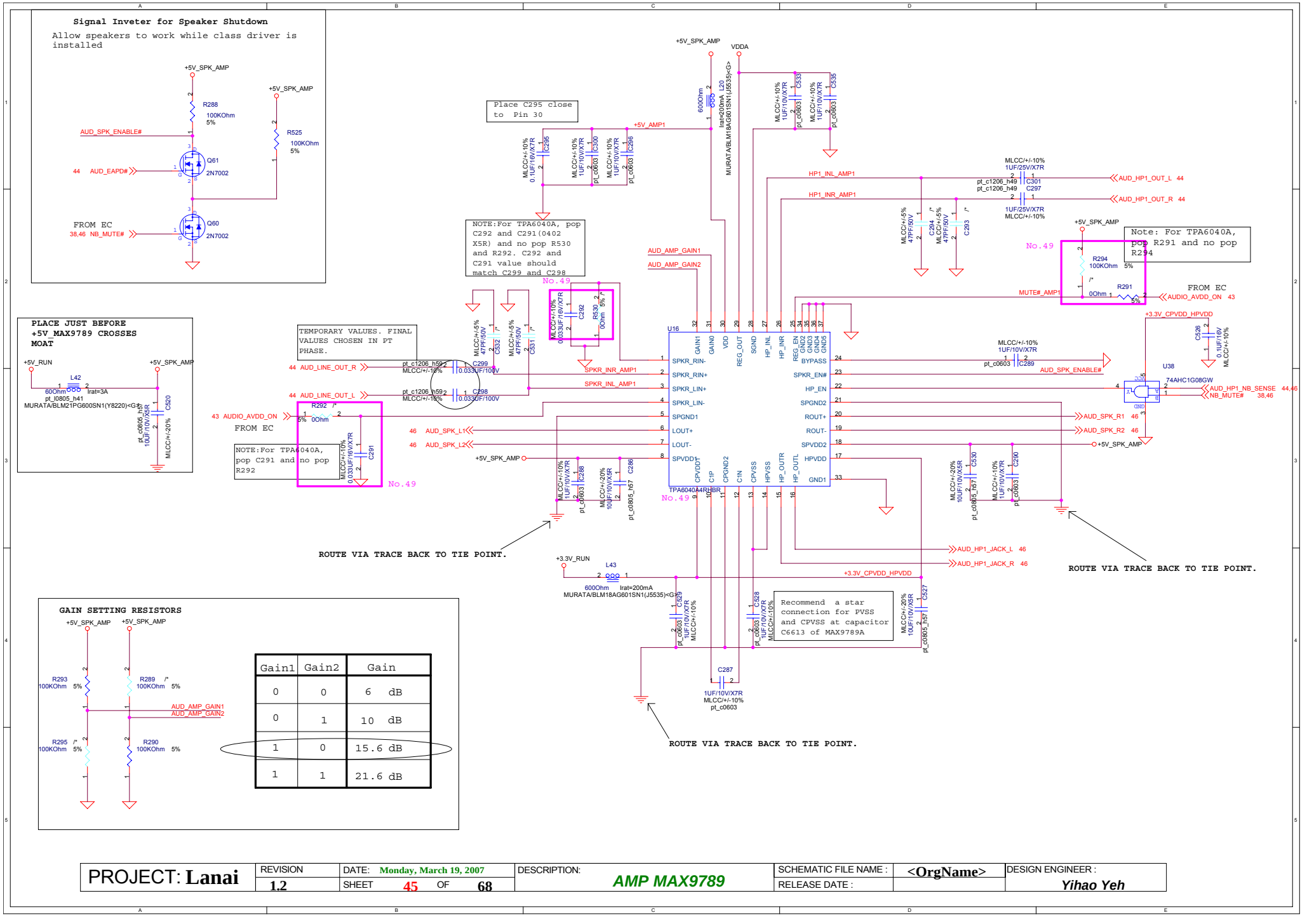
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***SWITCH & LED*** | SCHEMATIC FILE NAME : **<OrgName>** | DESIGN ENGINEER : ***C*** |
| | | SHEET **42** OF **68** | | RELEASE DATE : | |



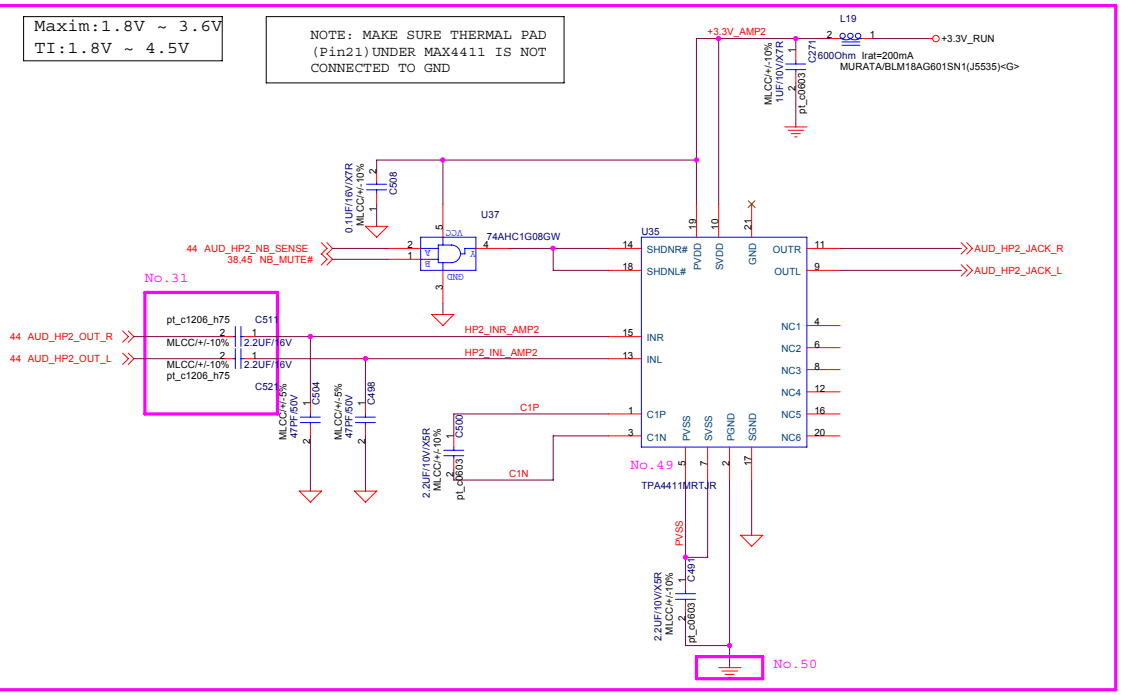



| PROJECT: Lanai | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | DESIGN ENGINEER : |
|---|---|---|---|---|---|
| | 1.2 | SHEET 44 OF 68 | STAC9228 | RELEASE DATE : | Yihao Yeh |

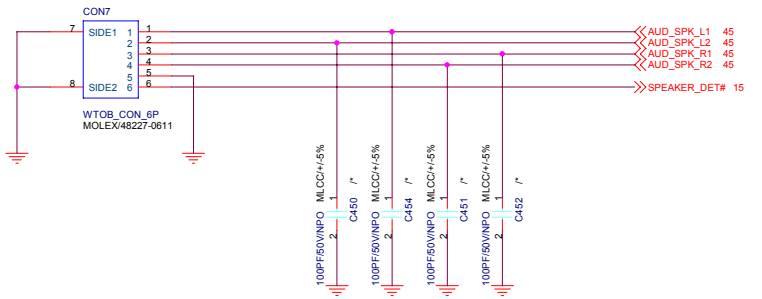


Maxim:1.8V ~ 3.6V
TI:1.8V ~ 4.5V

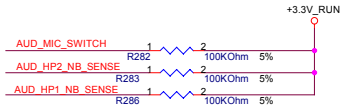
NOTE: MAKE SURE THERMAL PAD (Pin21)UNDER MAX4411 IS NOT CONNECTED TO GND

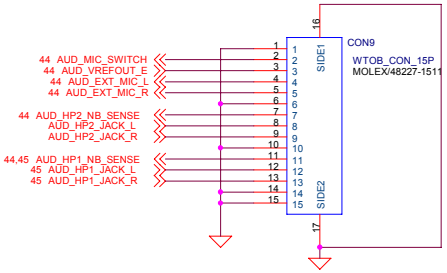



## Speaker CON

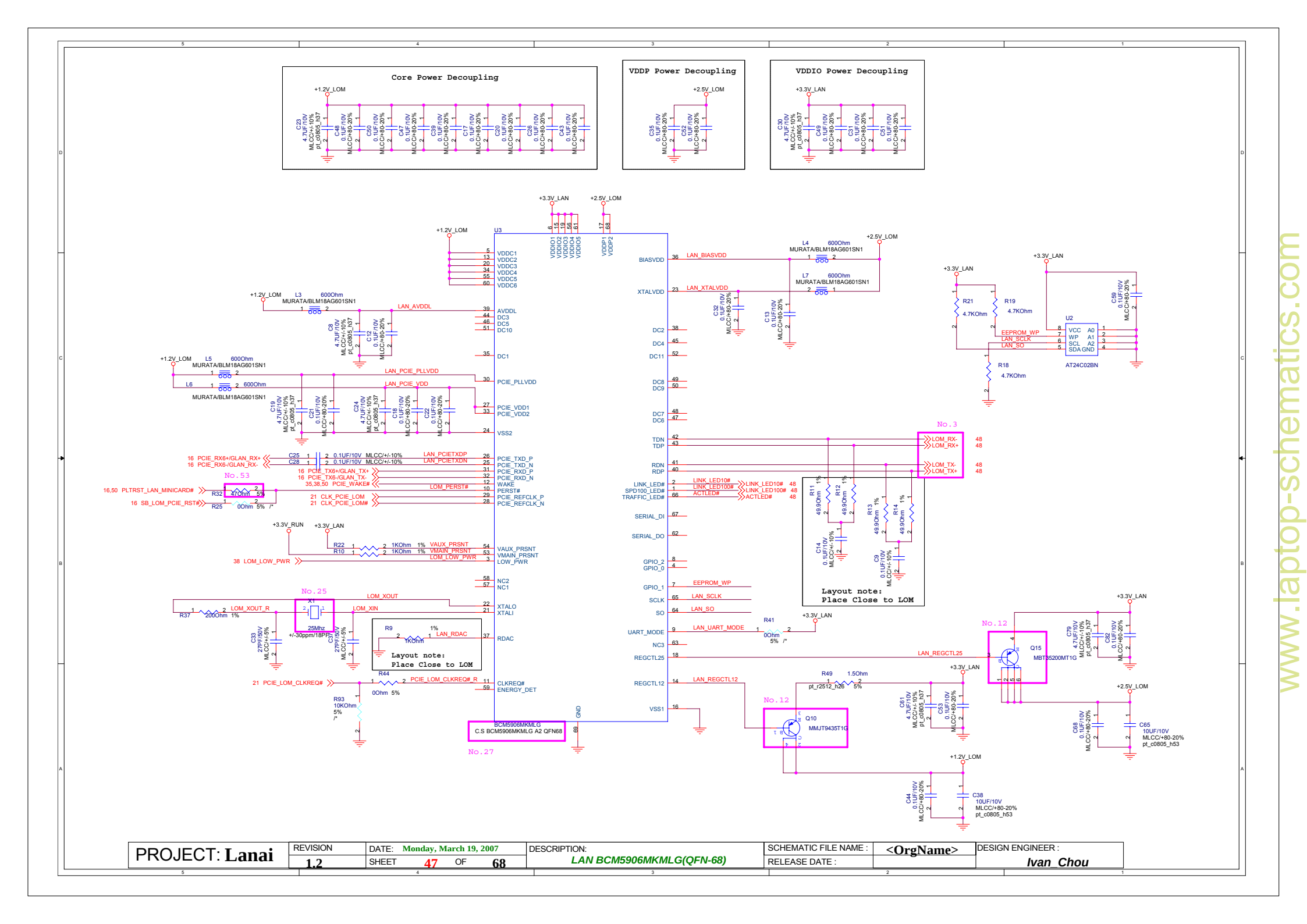



Need to adjust EMI cap values as necessary.




| PROJECT: Lanai | REVISION 1.2 | DATE: Monday, March 19, 2007 | DESCRIPTION: AMP MAX4411 & AUDIO JACK | SCHEMATIC FILE NAME : <OrgName> | DESIGN ENGINEER : Yihao Yeh |
|---|---|---|---|---|---|
| | | SHEET 46 OF 68 | | RELEASE DATE : | |

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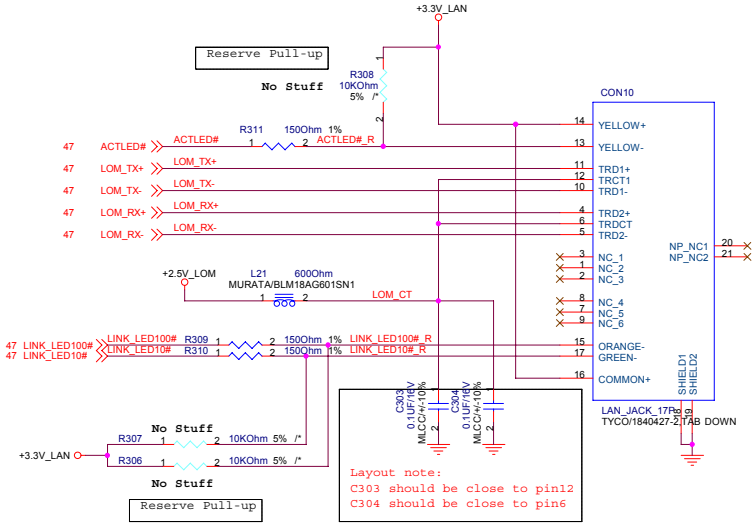
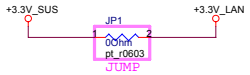
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***LAN BCM5906MKMLG(QFN-68)*** | SCHEMATIC FILE NAME : **<OrgName>** | DESIGN ENGINEER : ***Ivan_Chou*** |
| | | SHEET **47** OF **68** | | RELEASE DATE : | |




**+3.3V_LAN Source Guideline:**

1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on-LAN is required out of S4, S5

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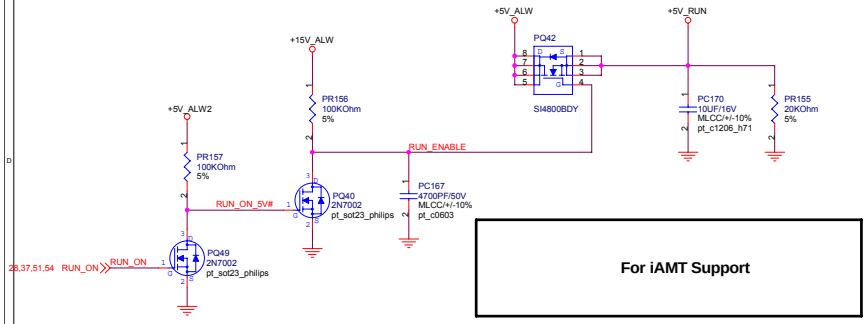
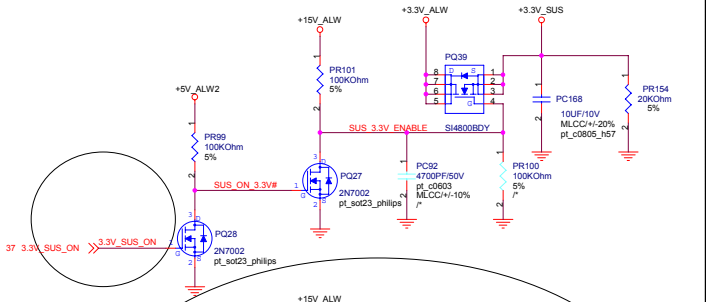
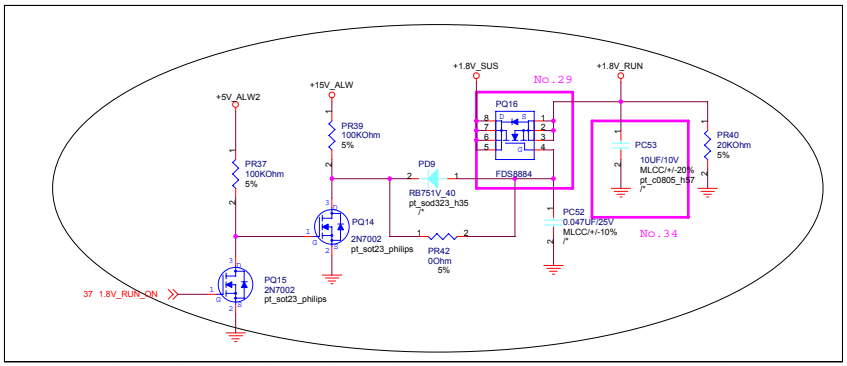
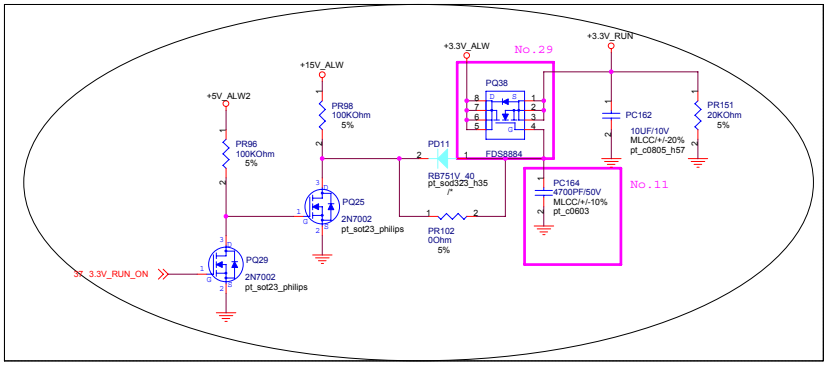
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: ***Magnetics and RJ-45*** | SCHEMATIC FILE NAME : | **<OrgName>** | DESIGN ENGINEER : ***Ivan_Chou*** |
| | | SHEET **48** OF **68** | | RELEASE DATE : | | |

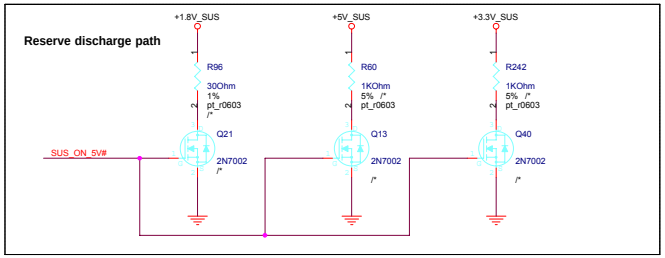


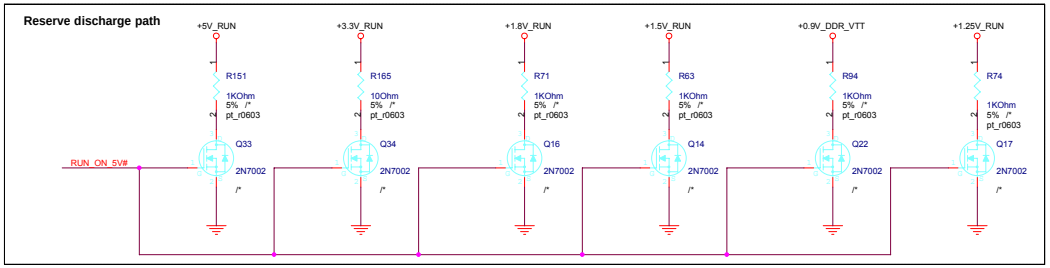

For iAMT Support



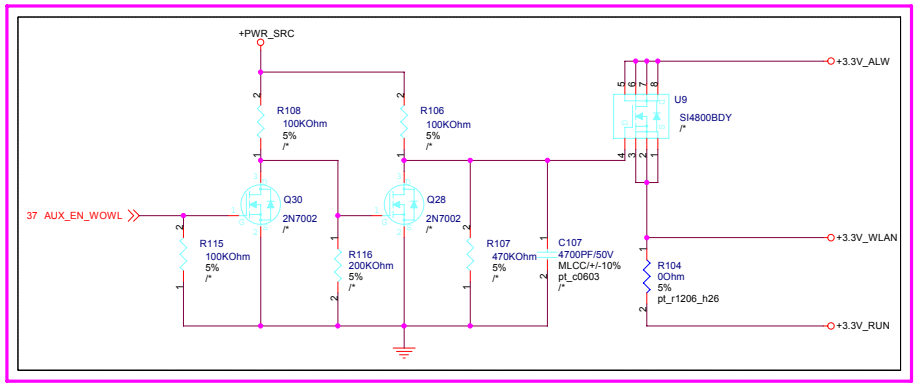



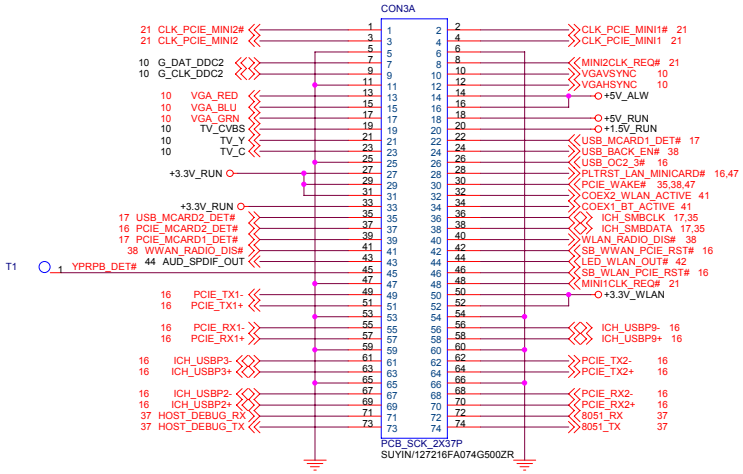



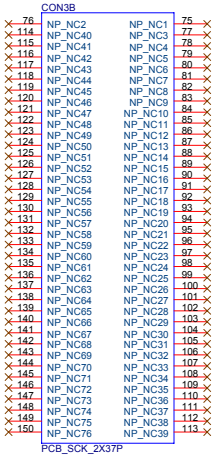

For iAMT Support

| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION: 1.2 | DATE: Monday, March 19, 2007 | DESCRIPTION: *Power Control Switch* | SCHEMATIC FILE NAME : | DESIGN ENGINEER : *Eric Ko* |
| | | SHEET 49 OF 68 | | RELEASE DATE : | |

No.21

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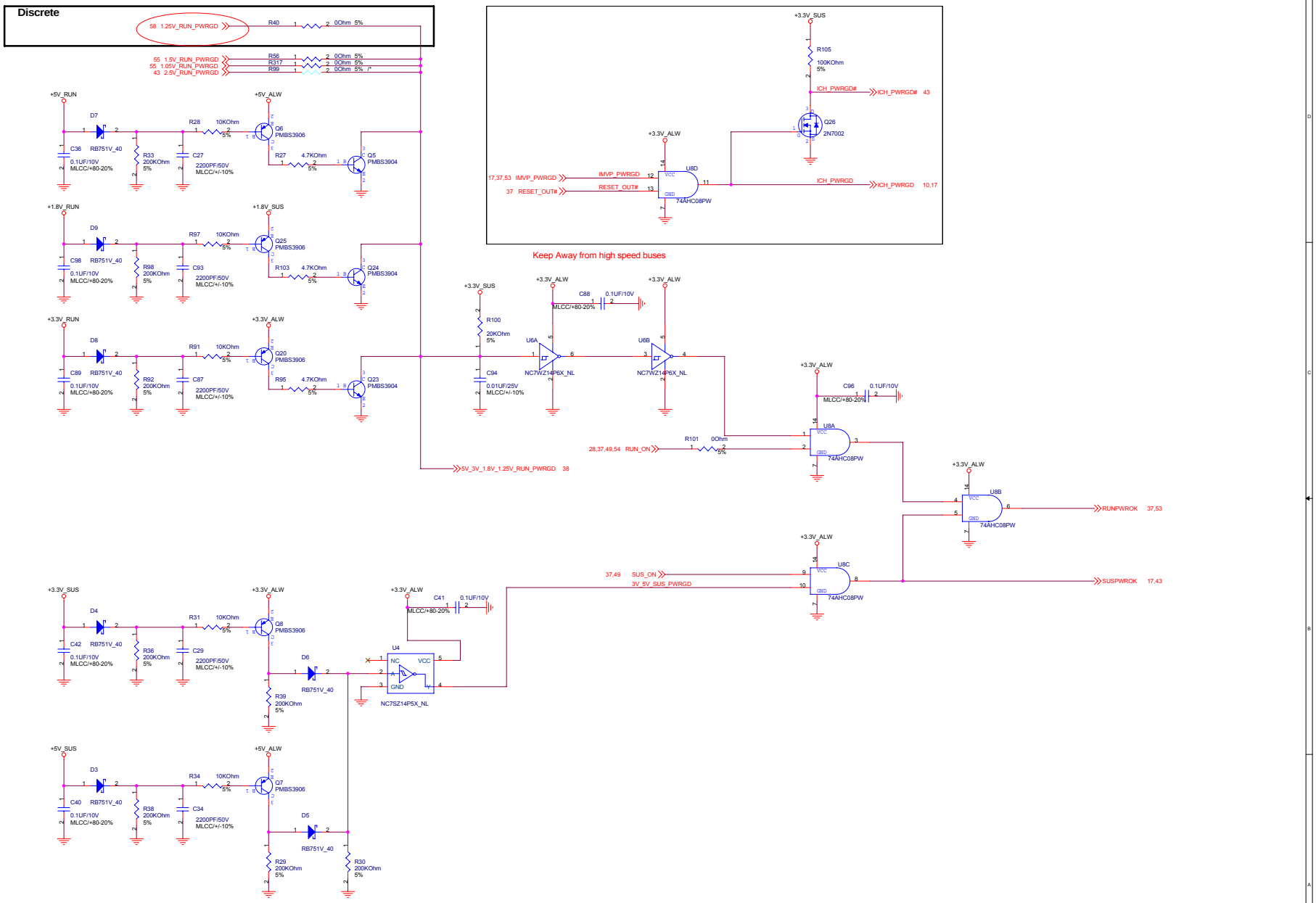
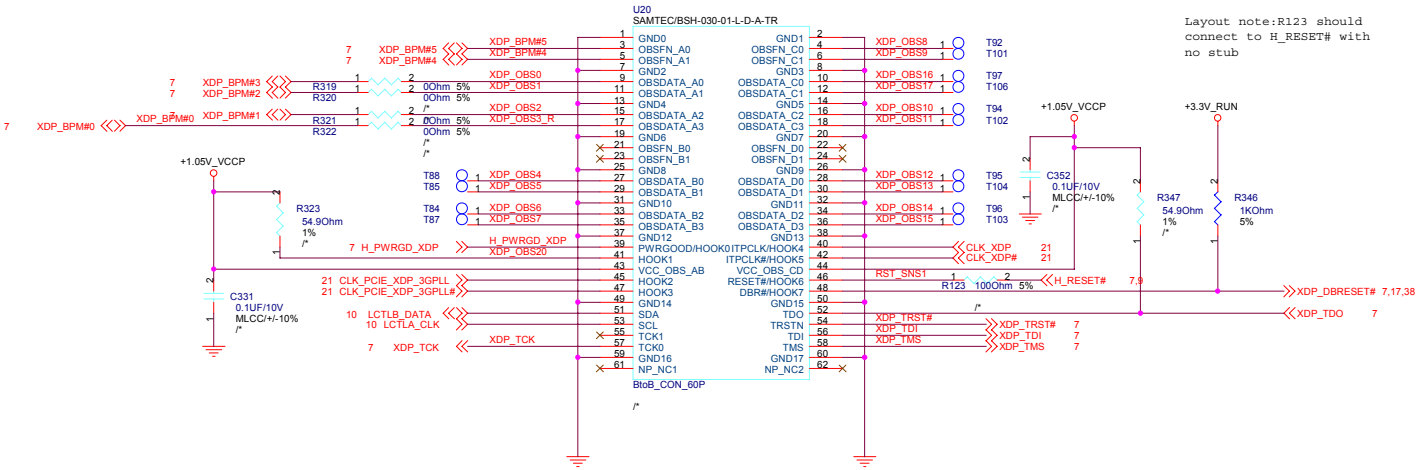
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***BtoB CON*** | SCHEMATIC FILE NAME : **<OrgName>** | DESIGN ENGINEER : ***STANLY_HSU*** |
| | | SHEET **50** OF **68** | | RELEASE DATE : | |

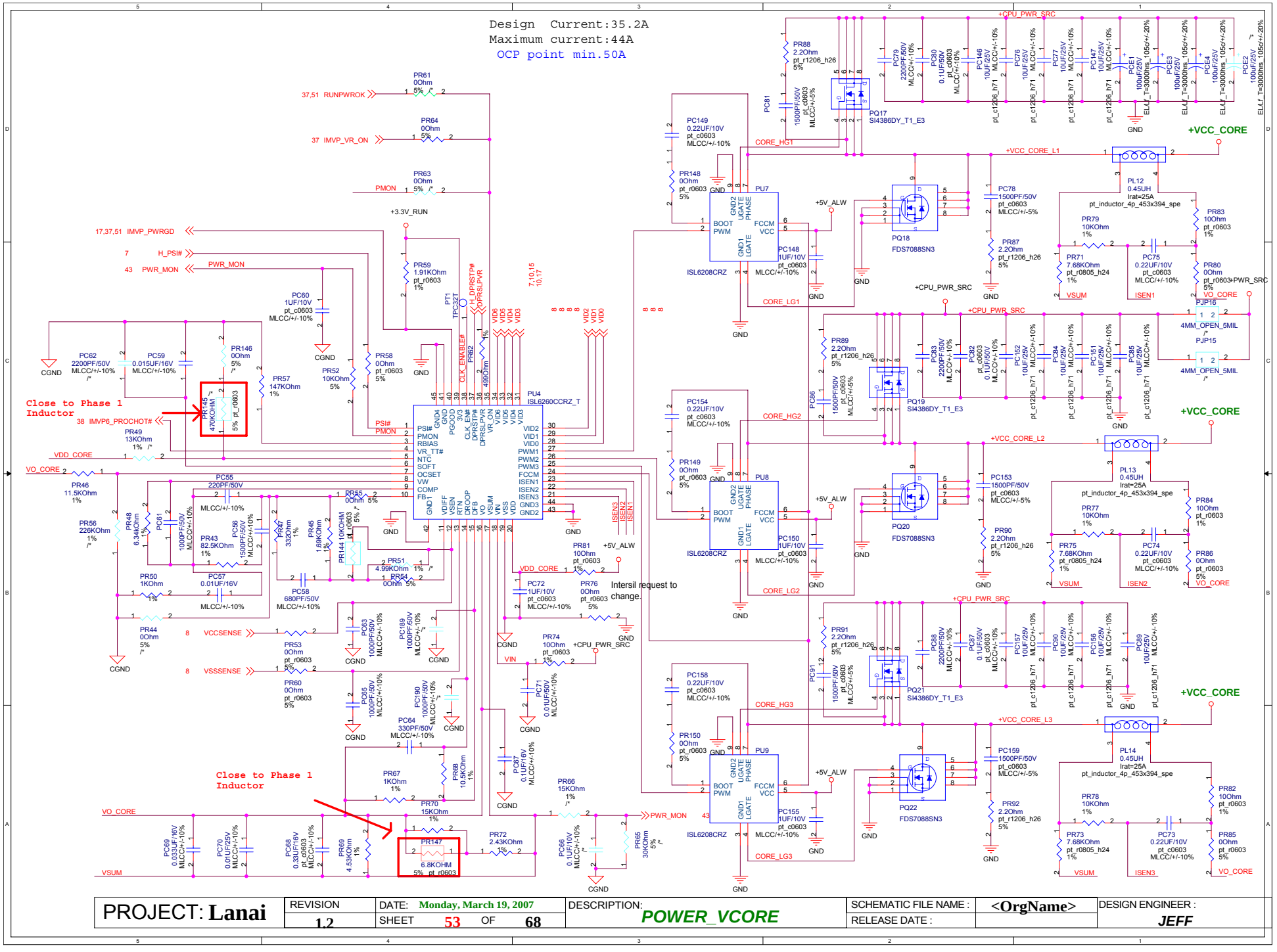


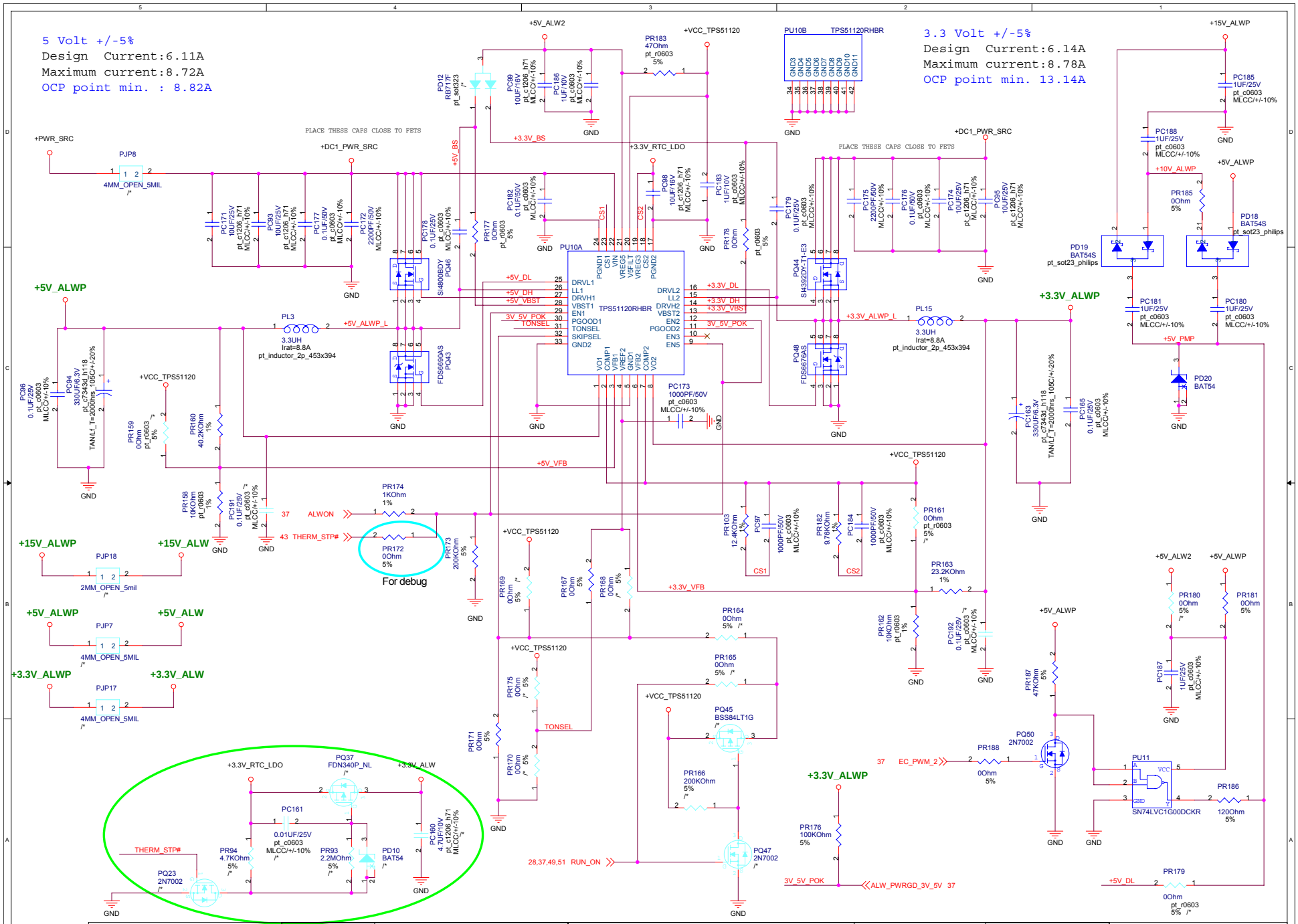

| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION: 1.2 | DATE: Monday, March 19, 2007 | DESCRIPTION: *Power Sequence Logic* | SCHEMATIC FILE NAME : | DESIGN ENGINEER : *C.L. Ho* |
| | | SHEET 51 OF 68 | | RELEASE DATE : | |

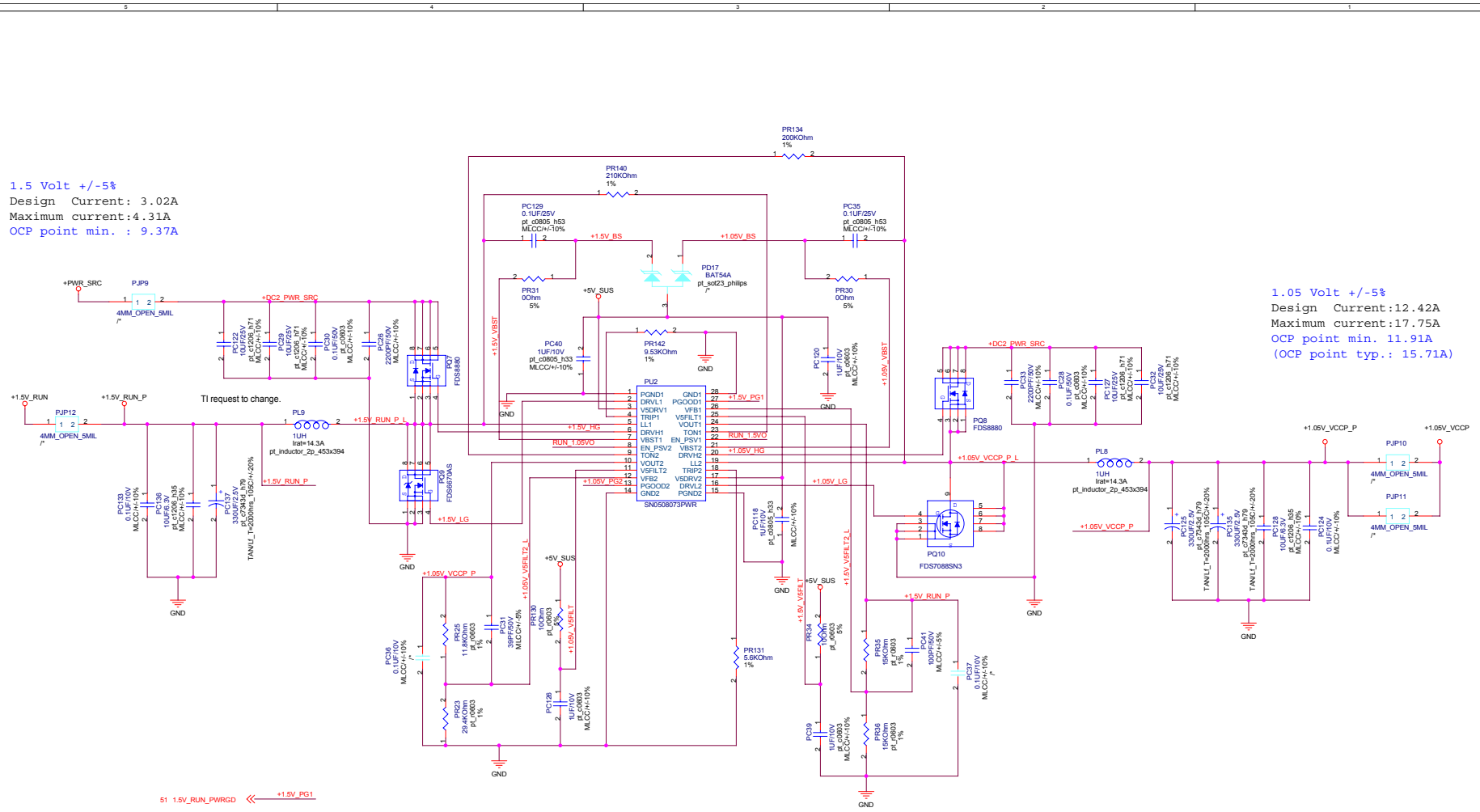
# XDP




| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***XDP*** | SCHEMATIC FILE NAME : | **<OrgName>** | DESIGN ENGINEER : ***Terry_Lin*** |
| | | SHEET **52** OF **68** | | RELEASE DATE : | | |

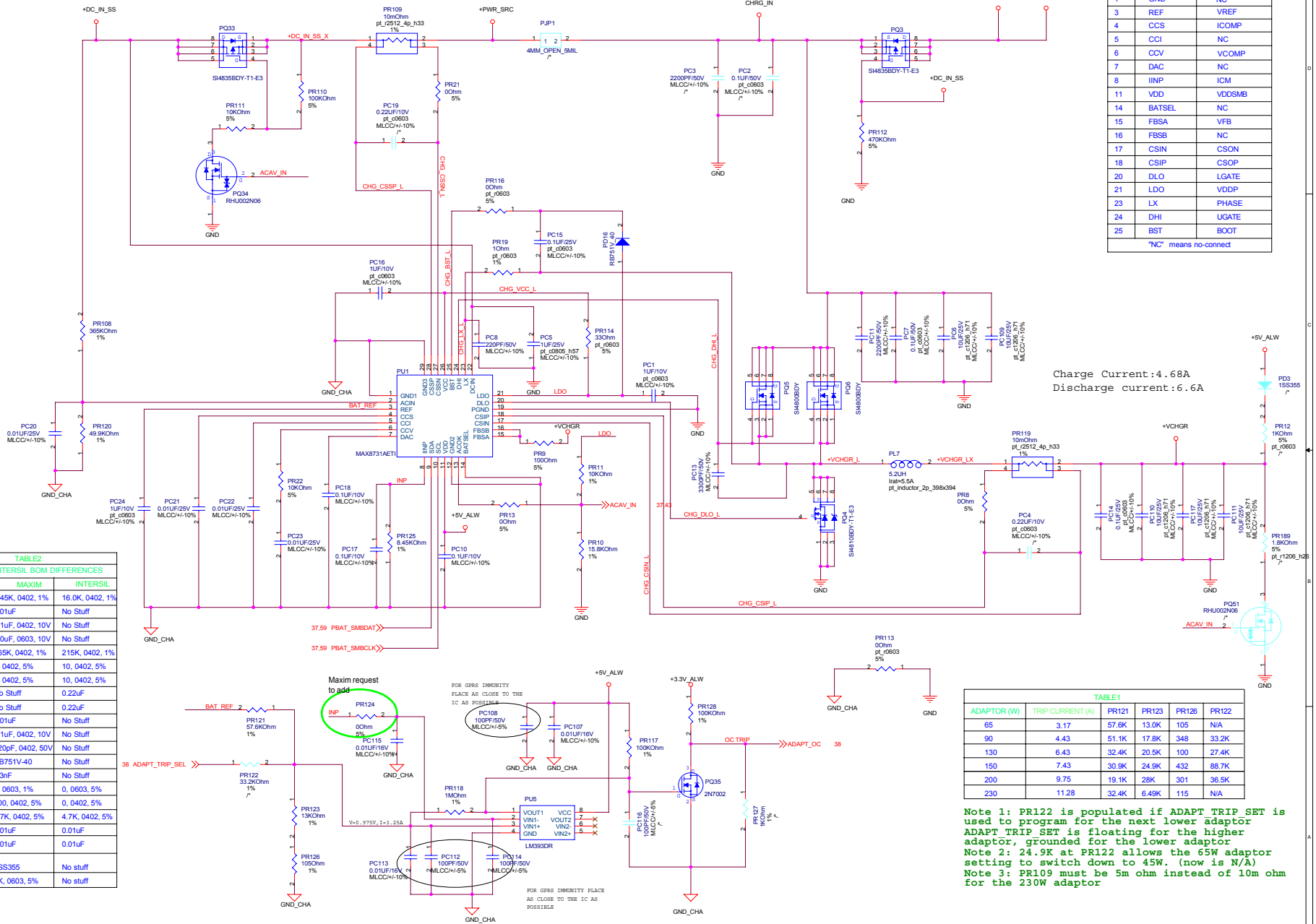







| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | 1.2 | SHEET 55 OF 68 | POWER I/O 1.5VS & 1.05VS | RELEASE DATE : | | JEFF |

TOTAL POWER=65W
-->3.34A



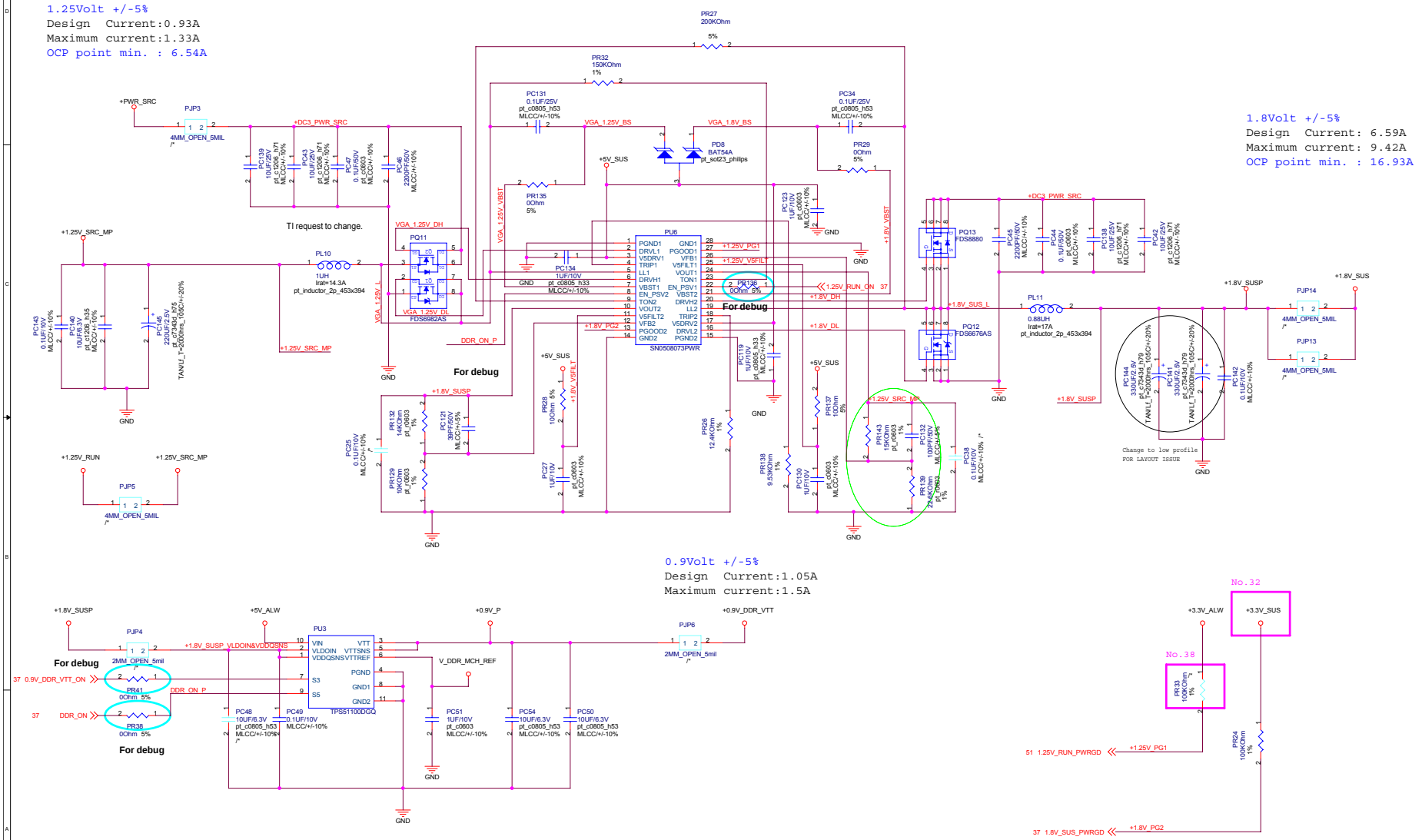

| TABLE3 | | |
|---|---|---|
| PIN NAME DIFFERENCES | | |
| PIN | MAXIM | INTERSIL |
| 1 | GND | NC |
| 3 | REF | VREF |
| 4 | CCS | ICOMP |
| 5 | CCI | NC |
| 6 | CCV | VCOMP |
| 7 | DAC | NC |
| 8 | IINP | ICM |
| 11 | VDD | VDDSMB |
| 14 | BATSEL | NC |
| 15 | FBSA | VFB |
| 16 | FBSB | NC |
| 17 | CSIN | CSON |
| 18 | CSIP | CSOP |
| 20 | DLO | LGATE |
| 21 | LDO | VDDP |
| 23 | LX | PHASE |
| 24 | DHI | UGATE |
| 25 | BST | BOOT |
| "NC" means no-connect | | |

| TABLE2 | | |
|---|---|---|
| MAXIM & INTERSIL BOM DIFFERENCES | | |
| REF DES | MAXIM | INTERSIL |
| PR125 | 8.45K, 0402, 1% | 16.0K, 0402, 1% |
| PC115 | 0.01uF | No Stuff |
| PC17 | 0.1uF, 0402, 10V | No Stuff |
| PC24 | 1.0uF, 0603, 10V | No Stuff |
| PR108 | 365K, 0402, 1% | 215K, 0402, 1% |
| PR8 | 0, 0402, 5% | 10, 0402, 5% |
| PR21 | 0, 0402, 5% | 10, 0402, 5% |
| PC4 | No Stuff | 0.22uF |
| PC19 | No Stuff | 0.22uF |
| PC22 | 0.01uF | No Stuff |
| PC18 | 0.1uF, 0402, 10V | No Stuff |
| PC8 | 220pF, 0402, 50V | No Stuff |
| PD16 | RB751V-40 | No Stuff |
| PC13 | 3.3nF | No Stuff |
| PR19 | 1, 0603, 1% | 0, 0603, 5% |
| PR9 | 100, 0402, 5% | 0, 0402, 5% |
| PR22 | 4.7K, 0402, 5% | 4.7K, 0402, 5% |
| PC23 | 0.01uF | 0.01uF |
| PC21 | 0.01uF | 0.01uF |
| PD3 | 1SS355 | No stuff |
| PR12 | 1K, 0603, 5% | No stuff |

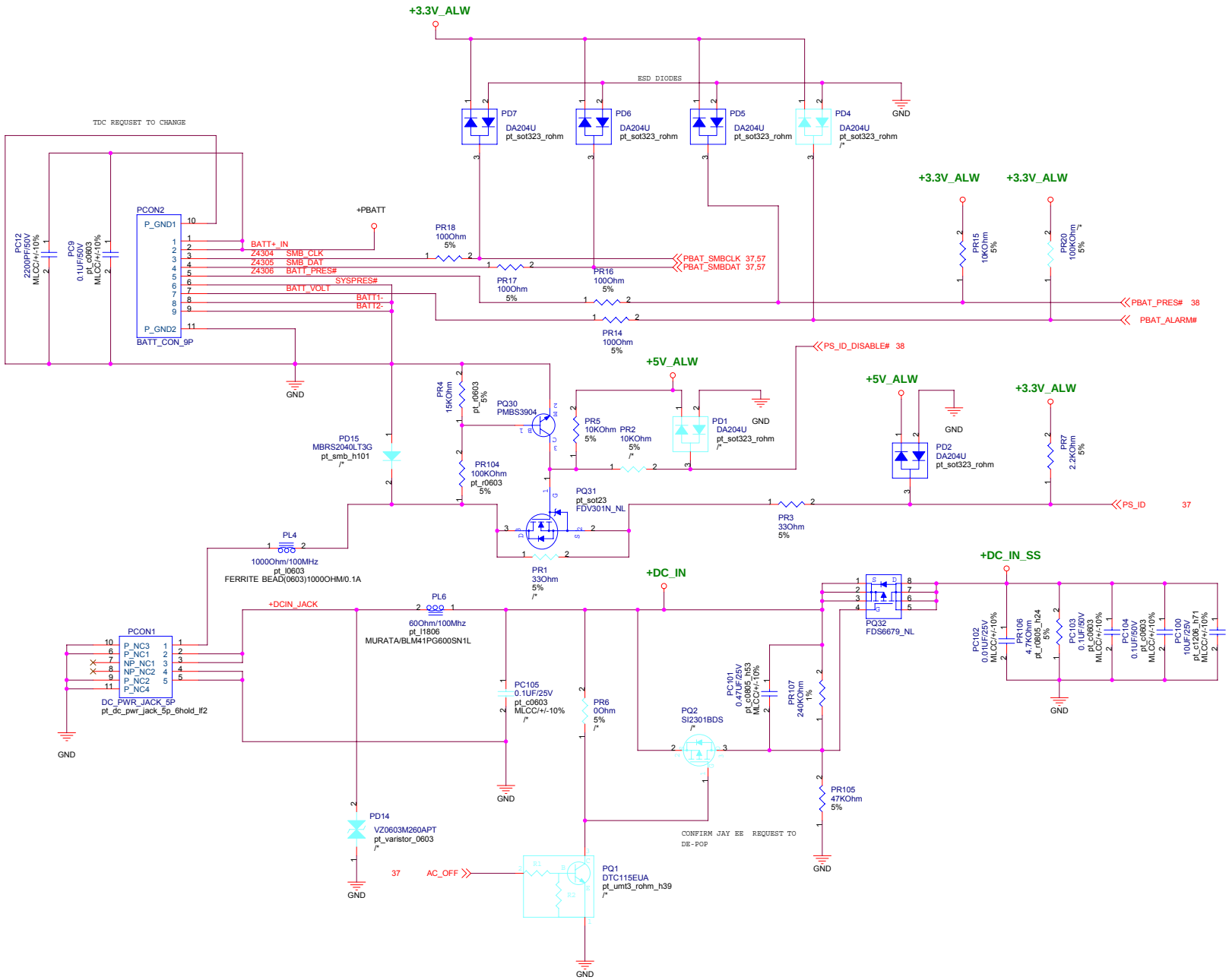
| TABLE1 | | | | | |
|---|---|---|---|---|---|
| ADAPTOR (W) | TRIP CURRENT (A) | PR121 | PR123 | PR126 | PR122 |
| 65 | 3.17 | 57.6K | 13.0K | 105 | N/A |
| 90 | 4.43 | 51.1K | 17.8K | 348 | 33.2K |
| 130 | 6.43 | 32.4K | 20.5K | 100 | 27.4K |
| 150 | 7.43 | 30.9K | 24.9K | 432 | 88.7K |
| 200 | 9.75 | 19.1K | 28K | 301 | 36.5K |
| 230 | 11.28 | 32.4K | 6.49K | 115 | N/A |

Note 1: PR122 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR122 allows the 65W adaptor setting to switch down to 45W. (now is N/A)
Note 3: PR109 must be 5m ohm instead of 10m ohm for the 230W adaptor

| PROJECT: Lanai | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | DESIGN ENGINEER : |
|---|---|---|---|---|---|
| | 1.2 | SHEET 57 OF 68 | POWER_CHARGER | RELEASE DATE : | JEFF |

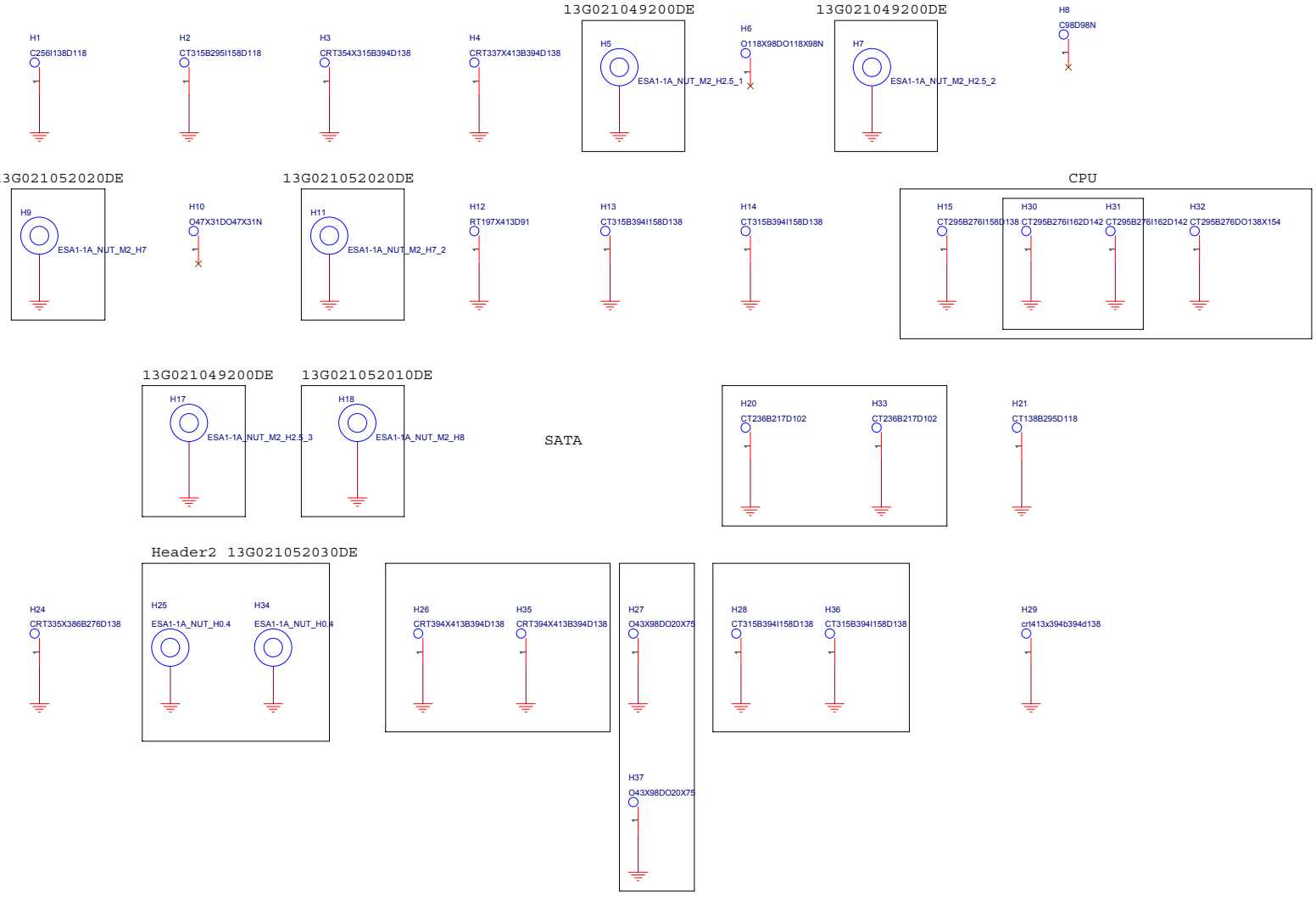



| PROJECT: Lanai | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : |
|---|---|---|---|---|---|---|
| | 1.2 | SHEET 58 OF 68 | POWER_VGA_1.25V & DDR & VTT | RELEASE DATE : | | Jeff |




| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION: **1.2** | DATE: **Monday, March 19, 2007** | DESCRIPTION: ***POWER_CONNECTOR*** | SCHEMATIC FILE NAME: **<OrgName>** | DESIGN ENGINEER: ***JEFF*** |
| | | SHEET **59** OF **68** | | RELEASE DATE: | |

GM screw pad

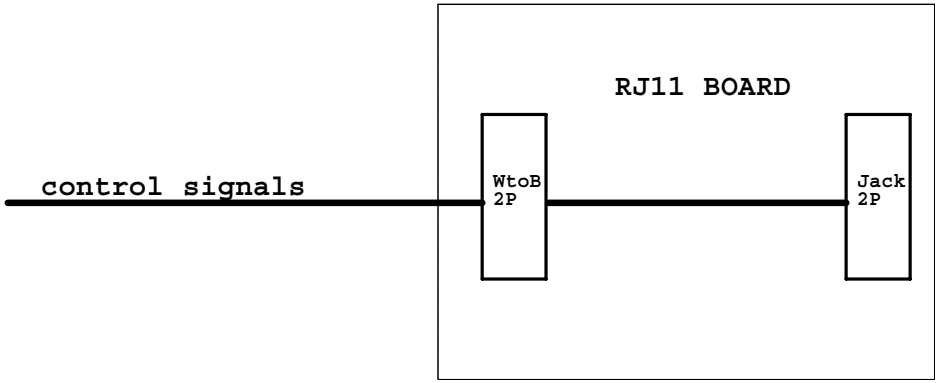



| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: ***SCREW PAD*** | SCHEMATIC FILE NAME : | DESIGN ENGINEER : ***Sean Kuo*** |
| | | SHEET **60** OF **68** | | RELEASE DATE : | |

# ASUS CONFIDENTIAL

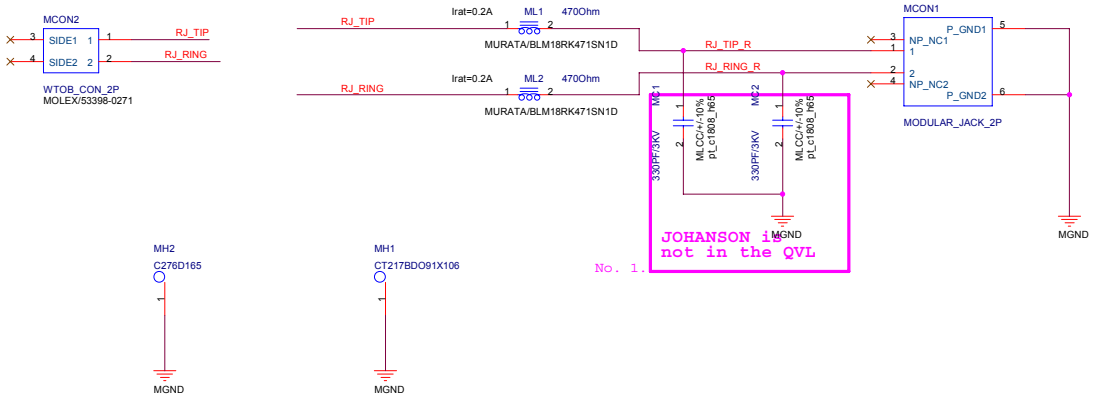
**MODEL NAME : *Elsa***

## *Lanai:Modem Board*




**REV : 1.1(DELL: X01)**

| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION: **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | DESIGN ENGINEER : |
| | | SHEET 64 OF 68 | ***BLOCK DIAGRAM*** | RELEASE DATE : | ***Stanly Hsu*** |




| | | | | | | |
|---|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: Monday, March 19, 2007 | DESCRIPTION: ***RJ-11 CONN*** | SCHEMATIC FILE NAME : | <OrgName> | DESIGN ENGINEER : ***Stanly_Hsu*** |
| | | SHEET 65 OF 68 | | RELEASE DATE : | | |

# ASUS CONFIDENTIAL

**MODEL NAME :** ***Elsa***

**PCB NO :** ***???***

**ASUS P/N :** ***???***

# Lanai PP2 USB Board

## REV : 1.1(DELL: X01)

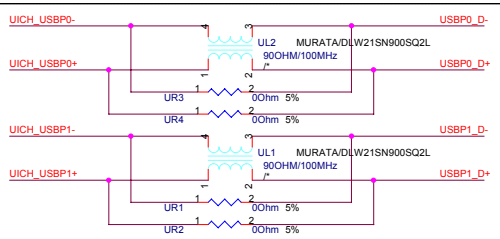
MB PCB

| Part Number | Description |
|---|---|
| DA800004H0L | PCB 00B LA-3071P REV0 M/B |

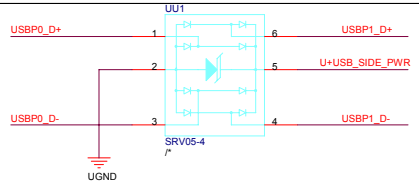
***BOM NO. ???***
***PCB P/N: ???***

| | | | | | |
|---|---|---|---|---|---|
| PROJECT: **Lanai** | REVISION **1.2** | DATE: **Monday, March 19, 2007** SHEET **67** OF **68** | DESCRIPTION: **Cover Page** | SCHEMATIC FILE NAME : RELEASE DATE : | DESIGN ENGINEER : ***Terry Lin*** |

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

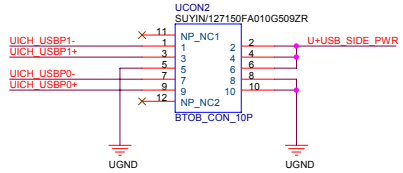



Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

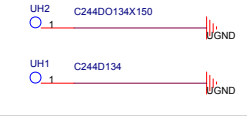



Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C ( 1pf vs 3pf ).

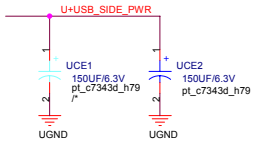
USB daughter board connector



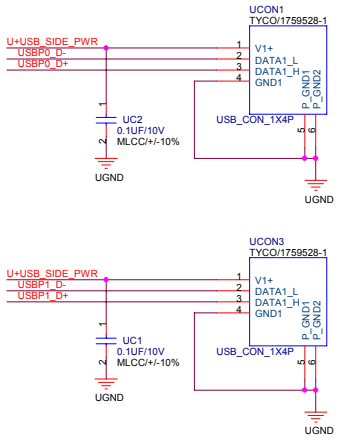

Screw hole




Place one 150uF cap by each USB connector




Each channel is 1A




Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.

| PROJECT: **Lanai** | REVISION | DATE: Monday, March 19, 2007 | DESCRIPTION: | SCHEMATIC FILE NAME : | DESIGN ENGINEER : |
|---|---|---|---|---|---|
| | 1.2 | SHEET 68 OF 68 | *USB PORT ( SINGLE * 2 )* | RELEASE DATE : | *Terry_Lin* |